

## PRODUCT SPECIFICATION

### Mini Cool Edge (MCIO) Connector for PCIe Series

DOCUMENT NUMBER:  
PS-0030

REVISION:  
AX03

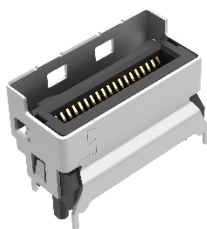
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Brown

APPROVED BY:  
James

DATE:  
10/07/2023

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### Mini Cool Edge (MCIO) Connector for PCIe 5.0/6.0 System



MCIO 4X-38Pos



MCIO 8X-74Pos



MCIO16X-124Pos

Rev.	Comments	Originator	Approval	Date
AX01	Initial	Brown	James Chen	04/12/2023
AX02	Add 4X and 16X Products	Brown	James Chen	07/07/2023
AX03	Add PCIe 6.0 series and Update Format	Brown	James Chen	10/07/2023

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## 1.0 SCOPE

This Product Specification covers performance, test, and reliability requirements of the [Zhaolong Mini Cool Edge \(MCIO\) Series connector for PCIe 5.0 /6.0 system](#).

## 2.0 PRODUCT DESCRIPTION

### PRODUCT NAME AND SERIES NUMBER(S)

- [02V1](#) Series: MCIO 8X-74Pos Vertical Connector for PCIe 5.0 Application
- [02V2](#) Series: MCIO 4X-38Pos Vertical Connector for PCIe 5.0 Application
- [02V3](#) Series: MCIO 16X-124Pos Vertical Connector for PCIe 5.0 Application
- [12V1](#) Series: MCIO 8X-74Pos Vertical Connector for PCIe 6.0 Application
- [12V2](#) Series: MCIO 4X-38Pos Vertical Connector for PCIe 6.0 Application
- [12V3](#) Series: MCIO 16X-124Pos Vertical Connector for PCIe 6.0 Application

### 2.1 DIMENSIONS, MATERIS, PLATINGS AND MARKING

- Housing
    - High temperature thermoplastic, UL94V-0
    - Color: Black
  - Contact
    - Copper Alloy
    - Contact area: Selected Gold plating
    - Solder area: Matte Tin plating
    - Under-plating: Nickel plating overall
  - Shell
    - Stainless steel
    - Solder area: Nickel under-plated
- See Customer Drawing for more information on dimensions, material, plating and marking.

### 2.2 ENVIRONMENTAL CONFORMANCE

See Customer Drawing for information on dimensions, material, plating and marking.

### 2.3 PIN ASSIGNMENTS

Pin assignment may vary depending on the cable assembly configuration. Different configurations will have different part numbers within the series. Refer to the appropriate cable sales drawing of the specific part number for the correct pin assignment.

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## **3.0 APPLICABLE DOCUMENTS AND SPECIFICATIONS**

### **3.1 INDUSTRY DOCUMENTS**

- EIA 364-1000 Environmental Test Methodology for Assessing the Performance of Connectors and Sockets Used in Controlled Environment Application
- EIA 364 Series Electrical Connector Test Procedures Including Environmental Classifications with Test Procedure
- PCI Express Card Electromechanical Specification 5.0 Rev 0.9
- Internal Cable Specification for PCI Express 5.0 and 6.0 Rev 0.7
- SFF-TA-1016 Internal Unshielded High Speed Connector System Rev 1.1
- SFF-TA-1024 Test Procedure for SFF-TA-1016 Mated Cable Assembly

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## 4.0 REQUIREMENT

### 4.1 DESIGN AND CONSTRUCTION RATING

Product shall be of the design, construction, material, and physical dimensions specified on the applicable product drawing.

### 4.2 RATING

- **Voltage:**  
30V DC Per Contact MAX
- **Current:**  
1.1 Amps Per Power Contact MAX  
1.1 Amps Per Contact MAX

Note: Ratings shown represent MAXIMUM current carrying capacity of a loaded connector with 12 circuits powered in still air. Ratings are based on a 30°C maximum temperature rise limit over ambient (room temperature 25°C). Current rating is application dependent. Appropriate de-rating is required depending on factors such as higher ambient temperature, gross heating from adjacent modules or components and other factors that influence connector performance.

- **Temperature**
  - Operating Temperature Range: - 40°C to + 85°C
  - Non-Operating Temperature Range: - 55°C to + 85°C
  - Field Temperature and Field Life: 65°C for 10 years (based on EIA-364-1000, Table C.1)

Note: Temperature life test duration (section 6.3.3) is based on the assumption that the contact spends its entire life at the rated field maximum temperature (based on EIA-364-1000, Table C.1).

- **Durability**
  - 200 Cycle for 0.76 µm Au. 10 Year Life (14-day MFG)
  - 100 Cycle for 0.38 µm Au. 10 Year Life (14-day MFG)

## 5.0 QUALIFICATION

Laboratory condition and sample selection are in accordance with EIA 364-1000

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## 6.0 PERFORMANCE AND TESTING

item	Test Description	Requirement	Test Produce
6.0.1	Visual & Dimensional inspection	Must meet the minimum requirements specified by product drawing.	EIA-364-18 Visual, dimensional, and functional inspection

### 6.1 ELECTRICAL PERFORMANCE

item	Test Description	Requirement	Test Produce
6.1.0	Current Rating	1.1A Per Contact MAX 1.1A Per Power Contact MAX	EIA-364-70 Apply a current of <b>100</b> mA maximum and voltage of <b>20</b> mv maximum. Ambient Conditions: Still air at 25 ±5°C
6.1.1	Low Level Contact Resistance (LLCR) (Initial)	Base line	EIA-364-23-Option 1 Apply a current of <b>100</b> mA maximum and voltage of <b>20</b> mv maximum
6.1.2	Low Level Contact Resistance (LLCR) (Change from Initial)	ΔR <b>20</b> milliohms maximum for signal contacts	EIA-364-23-Option 1 Apply a current of <b>100</b> mA maximum and voltage of <b>20</b> mv maximum
6.1.3	Dielectric Withstanding Voltage	No defect or breakdown No disruptive discharge Current leakage < <b>0.5</b> mA	EIA 364-20C – Method B Apply <b>300V</b> AC for <b>1</b> minute between adjacent terminals
6.1.4	Insulation Resistance	<b>1000</b> Megohms Minimum	EIA-364-21 Apply a voltage of <b>100V</b> DC for <b>1</b> minute between adjacent terminals and between terminals to ground

### 6.2 MECHANICAL PERFORMANCE

Item	Test Description	Requirement	Test Produce
6.2.1	Durability (Preconditioning)	No evidence of physical damage	EIA 364-09 Cycle rate: 500±50 per hour, Speed rate: 25.4 ±3mm/Minute Perform <b>20</b> mate/unmated cycles. Rate: 5 cycles per minute maximum
6.2.2	Durability	No evidence of physical damage	EIA 364-09 Cycle rate: 500±50 per hour, Speed rate: 25.4 ±3mm/Minute

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			Number of cycles: <b>200</b> cycles for 30μ" Au plating <b>100</b> cycles for 15μ" Au plating Replace mating cards after <b>25</b> cycles
6.2.3	<b>Mating Force (Module only)</b>	1.1N MAXIMUM per pin pair	EIA 364-13 - Method A Mate a <b>1.70 ±0.01</b> mm thickness gauge or AIC card to the connector at a rate of 25.4mm per minute
6.2.4	<b>Un-mating Force (Module only)</b>	0.1N MINIMUM per pin pair	EIA 364-13 -Method A Pull out a <b>1.44 ±0.01</b> mm thickness gauge or AIC card to at a rate of 25.4mm per minute
6.2.5	<b>Active Latch Retention Strength</b>	50 N MINIMUM	EIA 364-13 -Method A Rate: 25.4 mm/minute Pull in direction parallel to insertion, hold for minimum of 60 seconds
6.2.6	<b>Wrenching strength (W/ mated Cable- Passive Latch</b>	25 NMINIMUM	Bend cable 90° at minimum bend radius. Pull in 4 axis directions for round cable. Pull in 2 axis directions for flat cable. No damage to plug/ cable assembly.
6.2.7	<b>Wrenching strength (W/ mated Cable- Active Latch)</b>	40 N MINIMUM	Bend cable 90° at minimum bend radius. Pull in 4 axis directions for round cable. Pull in 2 axis directions for flat cable. No damage to plug/ cable assembly.
6.2.8	<b>Contact Normal Force</b>	0.49 N (50 grams) minimum at nominal	EIA-364-04 Rate: 25.4 mm/minute
6.2.9	<b>Vibration</b>	No evidence of physical damage No discontinuities of ≥ 1 microsecond ΔR <b>20</b> milliohms maximum for signal contacts	EIA-364-28, Test Condition VII, Condition D Random profile: a.) <b>5</b> Hz @ <b>0.01</b> g <sup>2</sup> /Hz to <b>20</b> Hz @ <b>0.02</b> g <sup>2</sup> /Hz (slope up) b.) <b>20</b> Hz to <b>500</b> Hz @ <b>0.02</b> g <sup>2</sup> /Hz (flat) Input acceleration is <b>3.13</b> g RMS <b>15</b> minutes per axis for all 3 axes on all samples. c.) Random control limit tolerance is ±3 dB
6.2.10	<b>Shock (Mechanical)</b>	No evidence of physical damage No discontinuities of ≥ 1 microsecond	EIA-364-27, Test Condition H Profile: Trapezoidal shock 50 g ±10%

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		$\Delta R$ 20 milliohms maximum for signal contacts	Duration: 11 milliseconds Velocity change: 170" per second $\pm 10\%$ Quantity: 3 drops in each of 6 directions. Total of 18 drops per connector
6.2.11	<b>Reseating</b>	No evidence of physical damage	EIA 364-09 Manually mate and unmated the connector with add-in card for 3 cycles Rate: 5 cycles per minute

### 6.3 ENVIRONMENTAL PERFORMANCE

Item	Test Description	Requirement	Test Produce
6.3.1	<b>Shock (Thermal)</b>	No evidence of physical damage $\Delta R$ 20 milliohms maximum for signal contacts	EIA 364-32, Method A, Table 2, Test Condition 1, Duration A-4 -55°C to 85°C, perform 5 cycles in mating Step: a.) -55 °C Duration 30 Minutes b.) Connector transfer time from cold to hot 5 MIN(Max) c.) 85 °C (+3/-0) Duration 30 Mini d.) Connector transfer time from hot to cold 5(min) MAX:
6.3.2	<b>Temperature Life (Preconditioning)</b>	No evidence of physical damage	EIA 364-17, Method A (without electrical load) Expose 72 hours at 105 $\pm 2^\circ\text{C}$
6.3.3	<b>Temperature Life</b>	No evidence of physical damage $\Delta R$ 20 milliohms maximum for signal contacts	EIA 364-17, Method A (without electrical load) Test Condition 2, Test Condition C Expose 120 hours at 105 $\pm 2^\circ\text{C}$
6.3.4	<b>Salt Spray</b>	No evidence of physical damage $\Delta R$ 20 milliohms maximum for signal contacts	EIA-364-26B Test condition: mated connector. a.) 5 $\pm$ 1% salt. b.) temperature :35+1/-2°C. c.) Duration: 48 hours.
6.3.5	<b>Solderability</b>	95% of immersed area must show no voids or pin holes.	J-STD-002E Test Method A1: Temp:245°C $\pm$ 5°C Immerse and withdraw at 1 mm- 5 mm, per second



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			and dwell for 5 +/-0.5 seconds, Leads and terminations shall have flux applied uniformly and to cover the surfaces to be tested.
6.3.6	<b>Cyclic Temperature &amp; Humidity</b>	No Damage $\Delta R$ 20 milliohms maximum for signal contacts	EIA 364-31B, a) Test condition: Method III without conditioning Cycle the connector between <b>25 °C ± 3 °C</b> at <b>80 %</b> ± 3% RH and <b>65 °C ± 3 °C</b> at <b>50 %</b> ± 3% RH. Ramp times should be <b>0.5</b> hour and dwell times should be <b>1.0</b> hour. b) Test Duration: <b>24</b> hours per cycle c) Number of cycles: Perform <b>24</b> continuous cycles.
6.3.7	<b>Porosity Testing</b>	No Damage	Tested in accordance with EIA 364-53, minimum of 10 contacts from 3 samples must be tested, optical microscope of 10X magnification concentrated reagent grade nitric acid: 75%+/-1% HNO3.
6.3.8	<b>Mixed Flowing Gas (MFG)</b>	No evidence of physical damage	EIA 364-65, Class IIA Exposure time per EIA 364-1000 – Table 4.1 Expose 14 days (for 10-Year field life) in MFG chamber. Cl2: 10±3 ppb NO2: 200±50 ppb H2S: 10±5 ppb SO2: 100±20 ppb Temperature: 30±1°C
6.3.9	<b>Thermal Disturbance</b>	No evidence of physical damage	EIA 364-1000 – Table 4 Cycle the connector between <b>15 ±3°C</b> and <b>85 ±3°C</b> , as measured on the part. Ramp rate shall be an average <b>2°C</b> per minute. The minimum dwell time shall be <b>5</b> minutes after the specimens reached the chamber temperature. No humidity control. Perform <b>10</b> cycles
6.3.10	<b>Temperature Rise</b>	Maximum Temperature rise shall not exceed <b>30°C</b> above ambient.	EIA 364-70 Method 3 Maximum of 6 adjacent pins per side and 12 pins in total are connected in series.

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			A thermocouple is placed as close as possible to the contact interface Supply the rated current for a duration of 1 hour before measurement is taken. The ambient condition is still air at 25°C
6.3.11	<b>Resistance to soldering heat (Infrareds reflow)</b>	No evidence of physical damage	EIA-364-56 Procedure 6 Average ramp rate: 1~4°C per second Test Level 3: Temperature (board surface): 250 +10°C /-0°C Duration:30~35 seconds

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## 7.0 HIGH SPEED CHARACTERIZATION

### 7.1 SI PERFORMANCE FOR PCIE 5.0 APPLICATION

Item	Test Description	Requirement	Test Produce
1	<b>Insertion Loss (SDD21)</b>	$> -0.1-0.040625*f(\text{GHz}), 0 \leq f(\text{GHz}) \leq 16$ $> -1.75-0.15625*f(\text{GHz}), 16 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.1).
2	<b>Return Loss (SDD11/SDD22)</b>	$\leq -20+0.3125*f(\text{GHz}), 0 \leq f(\text{GHz}) \leq 16$ $\leq -35+1.25*f(\text{GHz}), 16 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.2)
3	<b>integrated Return Loss (iRL)</b>	$iRL \leq -26 \text{ dB}$ (Trise=25 ps) If DUT return loss violates the specified frequency-domain mask line over the 0-24 GHz range, use the iRL Metric.	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.2)
4	<b>Near-End Crosstalk (PSNEXT)</b>	$\leq -60+0.625*f(\text{GHz}) \text{ dB}, 0 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.3)
5	<b>Component Contribution ICN (ccICN PSNEXT)</b>	$\leq 450 \mu\text{V}$ Post-channel loss =-6dB at 16GHz If DUT PSNEXT violate the specified frequency-domain mask line over the 0-24 GHz range, use the cclCN Metric	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.3)
6	<b>Far-End Crosstalk (PSFEXT)</b>	$\leq -55+0.625*f(\text{GHz}), 0 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.4)
7	<b>Component contribution ICN (ccICN PSFEXT)</b>	$\leq 250 \mu\text{V}$ Post-channel loss =-6dB at 16GHz Pre-channel loss =-29dB at 16GHz If DUT PSFEXT violate the specified frequency-domain mask line over the 0-24 GHz range, use the cclCN Metric	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.4)

### 7.2 SI PERFORMANCE FOR PCIE 6.0 APPLICATION

Item	Test Description	Requirement	Test Produce
1	<b>Insertion Loss (SDD21)</b>	$> -0.1-0.025*f(\text{GHz}), 0 \leq f(\text{GHz}) \leq 16$ $> 0.5-0.00625*f(\text{GHz}), 16 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.1).
2	<b>Return Loss (SDD11/SDD22)</b>	$\leq -25+0.625*f(\text{GHz}), 0 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.2)
3	<b>integrated Return Loss (iRL)</b>	$\leq -31 \text{ dB}$ (Trise=25 ps) If DUT return loss violates the specified	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.2)

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		frequency-domain mask line over the 0-24 GHz range, use the iRL Metric.	
4	<b>Near-End Crosstalk (PSNEXT)</b>	$\leq -65 + 0.83333 \cdot f(\text{GHz}) \text{ dB}$ , $0 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.3)
5	<b>Component Contribution ICN (ccICN PSNEXT)</b>	ccICN $\leq 175 \mu\text{V}$ , Post-channel loss = -6dB at 16GHz If DUT PSNEXT violate the specified frequency-domain mask line over the 0-24 GHz range, use the ccICN Metric	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.3)
6	<b>Far-End Crosstalk (PSFEXT)</b>	$\leq -60 + 0.83333 \cdot f(\text{GHz})$ , $0 \leq f(\text{GHz}) \leq 24$	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.4)
7	<b>Component contribution ICN (ccICN PSFEXT)</b>	ccICN $\leq 150 \mu\text{V}$ Post-channel loss = -6dB at 16GHz Pre-channel loss = -25dB at 16GHz If DUT PSFEXT violate the specified frequency-domain mask line over the 0-24 GHz range, use the ccICN Metric	Internal Cable Specification for PCI Express 5.0 and 6.0 Version 0.7 (2.3.4)

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### 8.0 PRODUCT QUALIFICATION AND TEST SEQUENCE

Test or Examination		Test Groups														
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
6.0.1	Examination of connectors	1,8	1,10	1,10	1,12	1,9	1,3	1,7	1,5	1,3	1,3	1,3	1,3	1,3	1,3	1
6.1.1	Low Level Contact Resistance (LLCR)	2,5,7	2,5,7,9	2,5,7,9	2,5,7,9,11	4,6			2,4							
6.1.3	Dielectric Withstanding Voltage					2,7										
6.1.4	Insulation Resistance					3,8										
6.2.1	Durability (Preconditioning)	3	3	3	3											
6.2.2	Durability					5										
6.2.3	Mating Force (Module only)							3,6								
6.2.4	Un-mating Force (Module only)															
6.2.5	Active Latch Retention Strength										2					
6.2.6	Wrenching strength (W/ mated Cable-Passive Latch)												2			
6.2.7	Wrenching strength (W/ mated Cable-Active Latch)														2	
6.2.8	Contact Normal Force											2				
6.2.9	Vibration			6												
6.2.10	Shock (Mechanical)			8												
6.2.11	Reseating	6	8		10			2,5								
6.3.1	Shock (Thermal)		4													
6.3.2	Temperature Life (Preconditioning)			4	4											
6.3.3	Temperature Life	4						4								
6.3.4	Salt Spray								3							
6.3.5	Solderability									2						
6.3.6	Cyclic Temperature & Humidity		6													
6.3.7	Porosity Testing															2
6.3.8	Mixed Flowing Gas (MFG)				6											
6.3.9	Thermal Disturbance				8											
6.3.10	Temperature Rise					2										
6.3.11	Resistance to soldering heat (Infrared reflow)									2						
Sample Size		5	5	5	5	5	5	5	5	5	5	5	5	3	3	3

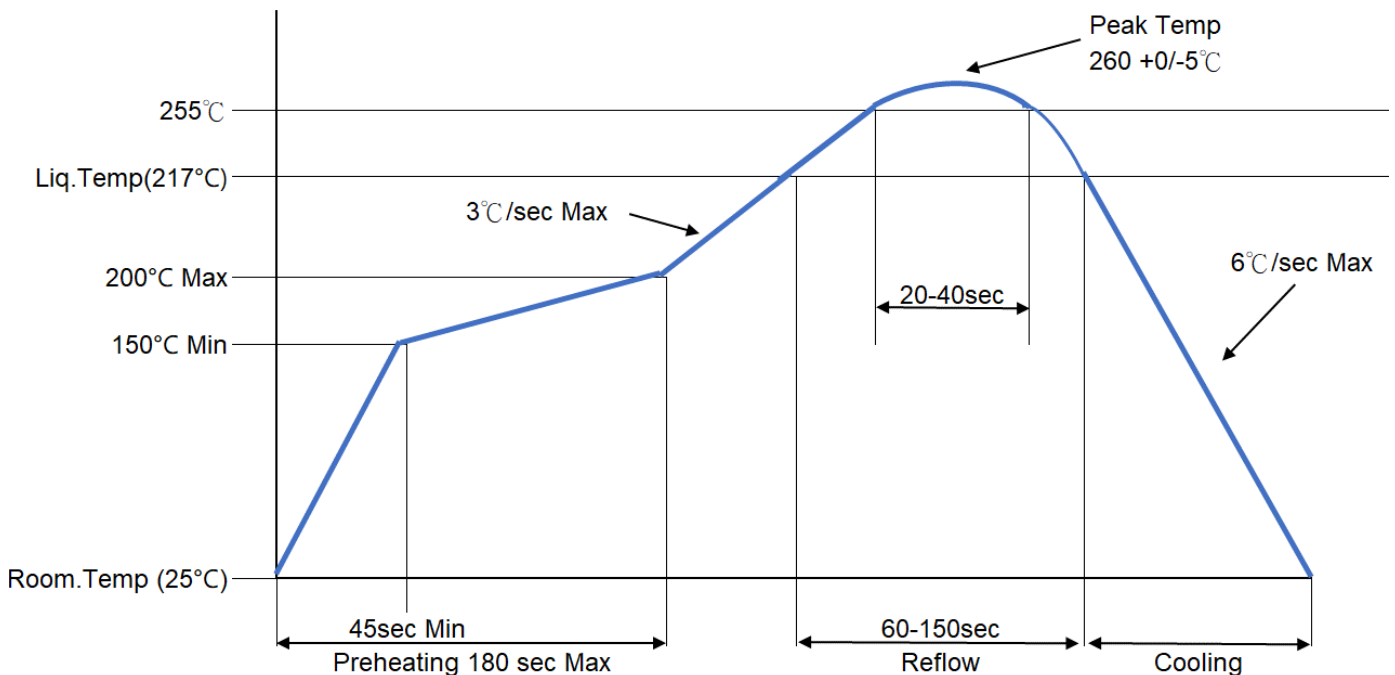
Note:

1. Test specimen: 5 PCS/ group unless otherwise specified.
2. Test specimen shall be sure to meet the drawing before the testing.

### 9.0 PACKING

Parts shall be packaged in Tape and Reel or Tray to protect against damage during handling, transit, and storage.

### 10.0 GNERIC LEAD-FREE REFLOW PROFILE



LEAD-FREE PROFIE FOR PEAK REFLOW **260°C**

#### Notes:

- Temperature indicated refers to the PCB surface temperature at solder tail area.
- Connector can withstand up to 2 reflow cycles with a cool-down to room temperature in-between.
- Actual reflow profile also depends on equipment, solder paste, PCB thickness, and other components on the board. Please consult your solder paste and reflow equipment manufacturer for their recommendations to adopt a suitable process.