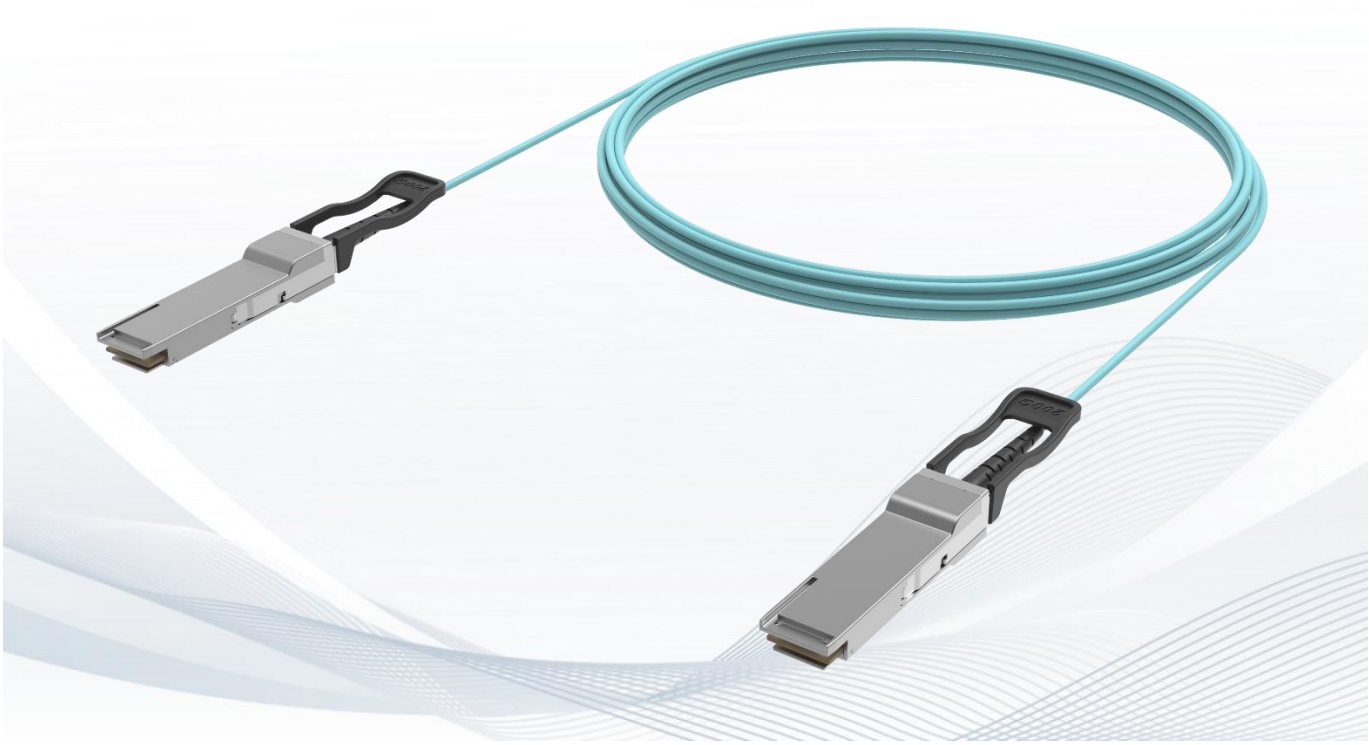


Application

- Data Center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test and Measurement Equipment
- 200Gb/s InifniBand HDR System
- Other Optical Link

Standards Compliance

- Compliant with QSFP56 MSA
- Compliant with IEEE 802.3bs
- Compliant with CMIS 5.0
- SFF-8417, SFF-8661, SFF-8679, SFF-8636

Highlight

- Up To 200Gb/S Data Rate
- 4x 50Gb/s PAM4 Modulation
- SFF-8665 Compliant QSFP56 Port
- SFF-8636 Compliant I2C Management
- Single 3.3V Power Supply
- 4.5W Power Dissipation Each End, With Retiming
- Operating Case Temp Commercial: 0°C To +70 °C
- Hot Pluggable
- RoHS Compliant

1.0 General Description

This datasheet pertains to the **200G QSFP56 to QSFP56 Active Optical Cable Assembly**, meticulously designed for application in the telecommunications and data center sectors. It facilitates bi-directional transmission of 200G traffic per cable, accommodating 4 lanes of 56G PAM4. The cable adheres to the standardized QSFP28(56) form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TST	-5		+75	°C	
Storage Relative Humidity	RH	5		85	%	
Maximum Supply Voltage	Vcc	-0.5		3.6	V	

2.2 Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typical	Max	Notes
Case Operating Temperature	TOP	°C	0	-	+70	Per End
Supply Voltage	Vcc	V	+3.13	+3.3	+3.47	
Bit Rate, per Lane	BR	GBd		26.5625		
Data Rate Accuracy	ΔDR	ppm	-100		+100	
Bit Error Rate (Pre-FEC)	BER				$2.4x10^{-4}$	
Power Consumption, per QSFP56	P	W			4.5	
Power-On Initialization Time		ms			2000	
Control Input Voltage High	VIH	V	2		Vcc+0.3	
Control Input Voltage Low	VIL	V	-0.3		0.8	
Control Output Voltage High	VOH	V	2		Vcc+0.3	
Control Output Voltage Low	VOL	V	-0.3		0.8	

Minimum Cable Bending Radius		mm	30			

Note1: Measured with a PRBS 231-1 test pattern @26.5625Gbd PAM4.

Note2: Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.

2.3 Electro-optical Characteristics

Parameters	Symbol	Unit	Min.	Typ.	Max.	Note
Transmitter						
Average Launch Power, per Lane	P_{AVG}	dBm	-6.0		+4.0	
Optical Wavelength, each Lane	λc	nm	840	850	860	
Spectral Width (RMS)	Δλ	nm			0.6	
Optical Extinction Ratio	ER	dB	3			
Optical Return Loss Tolerance	ORLT	dB			12	
Differential Data Input Voltage	V_{IN-PP}	mVpp	300		900	
Common Mode Noise RMS		mV			17.5	
Common Mode Voltage		V	-0.4		3.3	
Differential termination mismatch		%			10	
DC common mode voltage		mV	-350		2850	
Receiver						
Average Receive Power, per Lane	P_{Rx-AVG}	dBm	-7.9		+4.0	
Damage Threshold, per Lane	D_{TH}	dBm	+5.0			
Optical Wavelength, each Lane	λc	nm	840	850	860	
Receiver Reflectance	R_{Rx}	dB			-12	
Differential Data Output Voltage	V_{OUT-PP}	mVpp	300		900	
Differential termination mismatch		%			10	
Transition time (20% to 80%)	Tr, Tf	ps	9.5			
DC common mode voltage		mV	-350		2850	

2.4 Digital Diagnostic Specification

Parameter	Symbol	Accuracy	Units	Notes
Transceiver Case Temperature	DMI_TEMP	±5	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	±3	%	Full operating range
Channel Bias current monitor	DMI_IBIAS	±10	%	Per channel
Channel RX power monitor absolute error	DMI_RX	±3	dB	Per channel

2.5 Pin Assignments

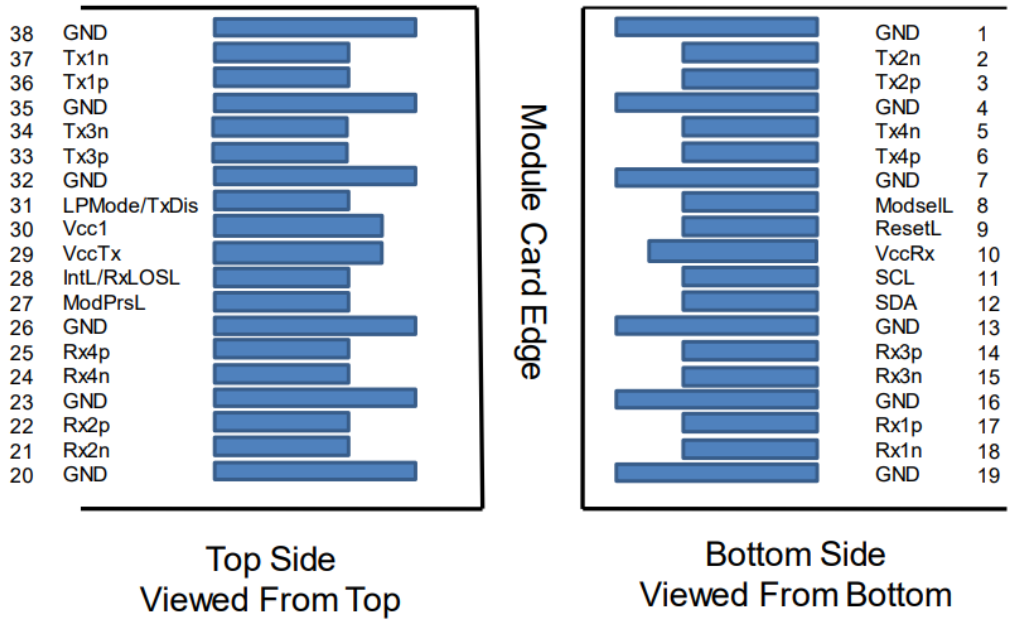


Figure 1 QSFP Module Contact Assignment

2.6 Pin Description

Table 1 QSFP28(56) Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-1	ModseIL	Module Select	3	
9	LVTTL-1	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface clock	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Present	3	
28	LVTTL-O	Int/RxLos	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 V Power supply transmitter	2	2
30		Vcc1	3.3 V Power supply	2	2
31	LVTTL-I	LPMode/Tx Dis	Low Power Mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1

36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1:
GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2:
VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.

2.7 Recommend Interface Circuit

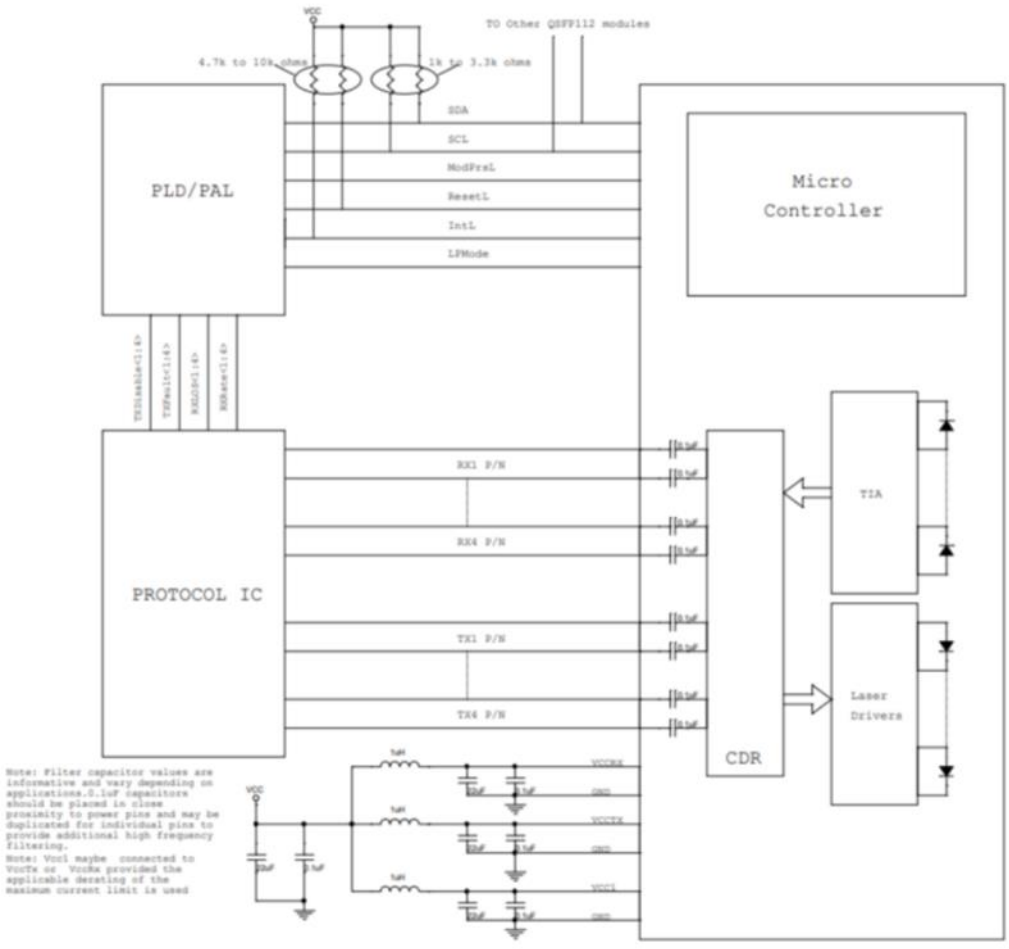


Figure 2 Recommend Interface Circuit

2.8 Memory Map information (SFF-8636 Version)

Table 2 SFF-8636 Memory Map

From	To	Content	No. of bytes	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	117	Free Side Device Properties	5	Read-Only
118	118	Reserved	1	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
Upper Page 00h				
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only

Note: For the above refer to **SFF-8636 Management Interface for 4-lane Modules and Cables Rev 2.10.2**

2.9 Memory Map information (CMIS Version)

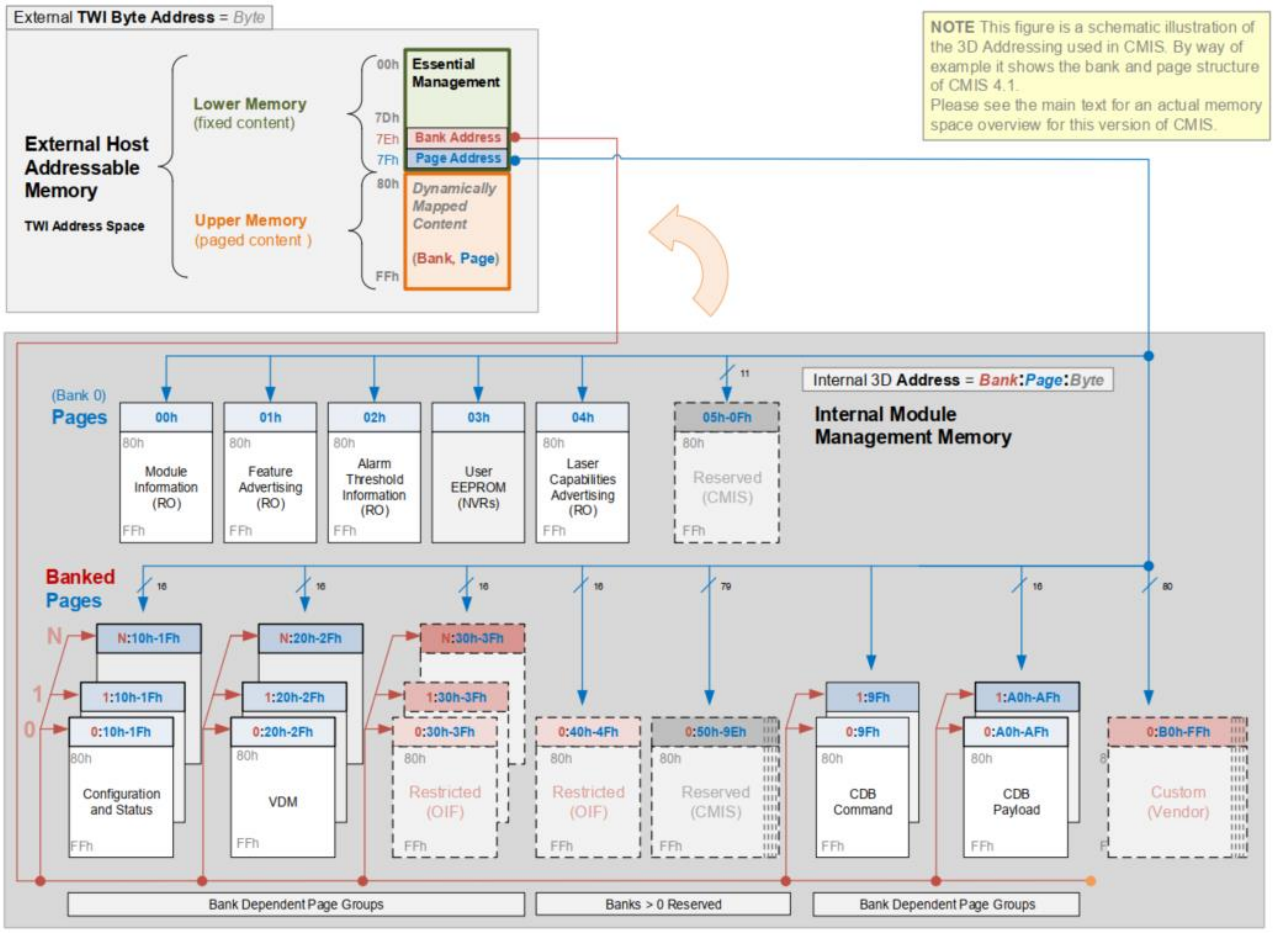


Figure 3 CMIS Module Memory Map (Conceptual View)

Table 3 CMIS Memory Map

■ Lower Memory Overview

Address	Size	Subject Area	Description
0-3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path spedific
26-3	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command

39-40	2	Module Firmware Version	Module Firmware Version
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s）
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII）
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Note: For the above, refer to **Common Management Interface Specification Rev5.0.**

2.10 Mechanical Specifications

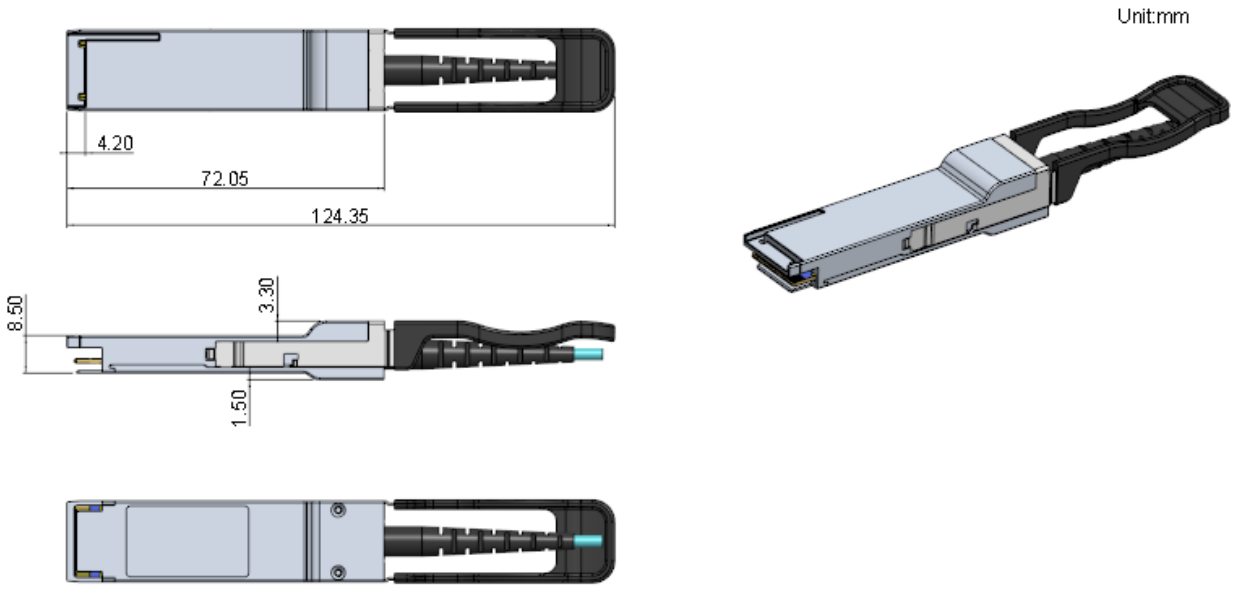
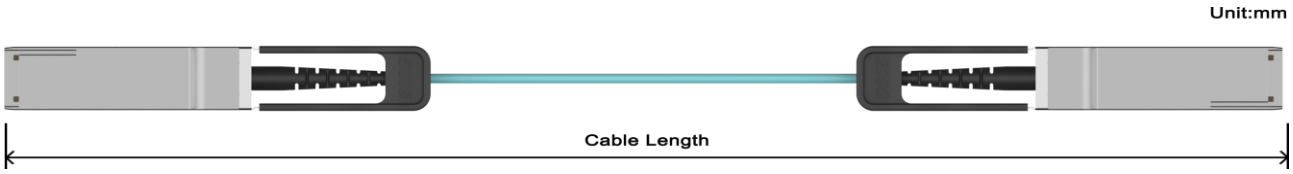


Figure 4 QSFP28(56) Form Factor

3.0 Product Information



■ Part Number System:

ZLAOC-A07- LLL-F-X

ZLAOC: Zhaolong Active Optical Cable Series.
A07: 200G QSFP56 to QSFP56 Active Optical Cable Assembly
LLL: Cable Length
3 Digits
Ex : 003=3m , 015=15m, 0p5=0.5m , 3p5=3.5m
F: Fiber Type
2:MM 50/125 OM2
3:MM 50/125 OM3*(Default)
4:MM 50/125 OM4
X Jacket Material:
P:PVC
Q:QFNP
L: LSZH*(Default)

Cable Length	Tolerance
<1m	+10/-0 cm
1~4.5m	+15/-0 cm
4.6m~14.5m	+30/-0 cm
14.6m~100m	+2%/-0 cm

■ ESD SAFETY CAUTIONS

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Important Notice

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4.0Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	10/01/2023