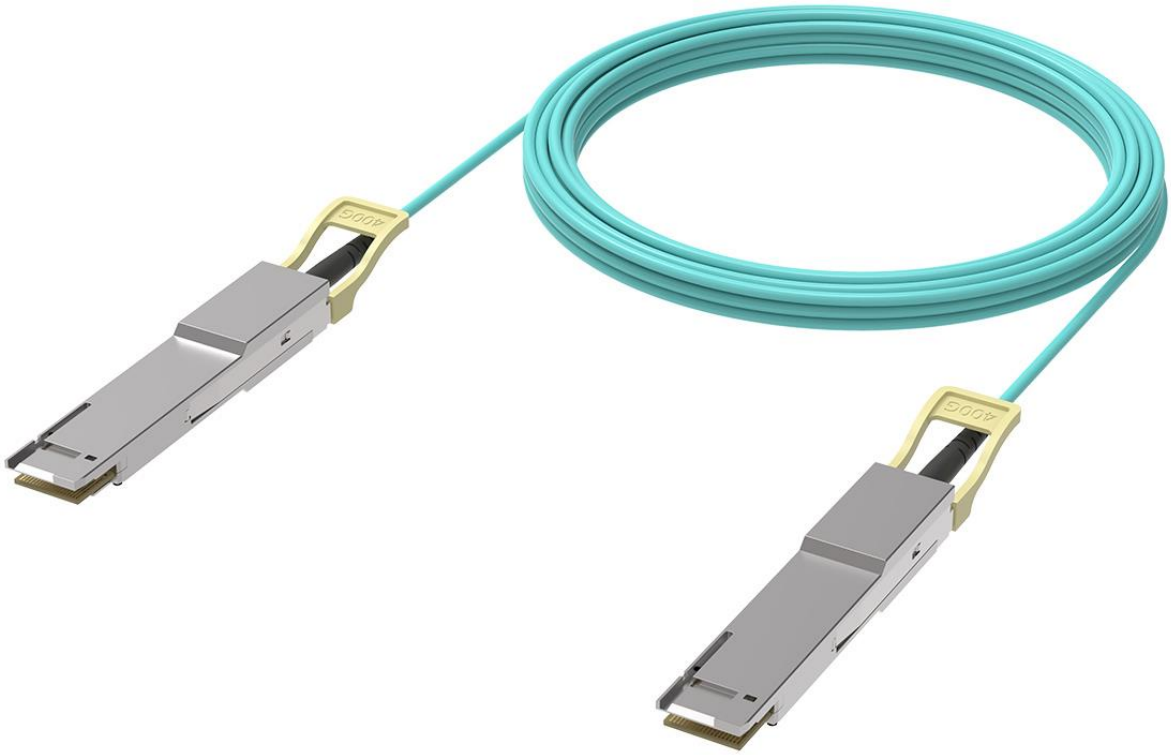
Product Datasheet

400G QSFP-DD Active Optical Cable



Application

- Data center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test and Measurement Equipment

Standards Compliance

- IEEE 802.3bs, IEEE 802.3cm
- QSFP-DD MSA Rev5.0
- CMIS4.0

Features

- Data rate up to 425Gb/s (8x PAM4 53Gb/s)
- 850nm VCSEL laser and PIN receiver
- High speed I/O electrical interface (400GAUI-8)
- Single +3.3V power supply
- Power consumption less than 10W per end
- Hot-pluggable QSFP-DD form factor
- Operating case temperature:0~+70°C
- Compliant to RoHS-10

1.0 Product Specification

1.1 Absolute Maximum Ratings (TC=25℃, unless otherwise noted)

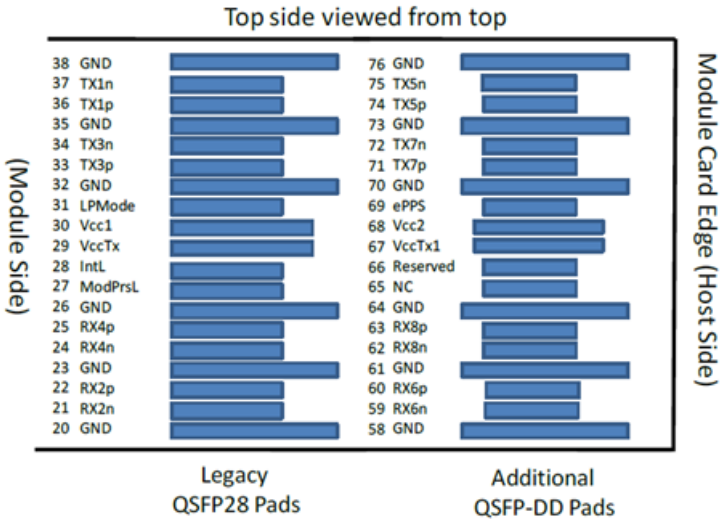
Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-10	-	+70	℃	
Maximum Supply Voltage	Vcc	-0.5	-	+3.6	V	
Operating Relative Humidity	RH	+15	-	+85	%	No condensation

1.2 General Specifications(TC=25℃, unless otherwise noted)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	Tc	0	-	70	℃	
Power Supply Voltage	Vcc	3.13	3.3	3.47	V	
Maximum Power Dissipation	P_D	-	-	10	W	
Lane Baud Rate	BR_{LANE}		53.125		Gbps	

1.3 PIN Descriptions



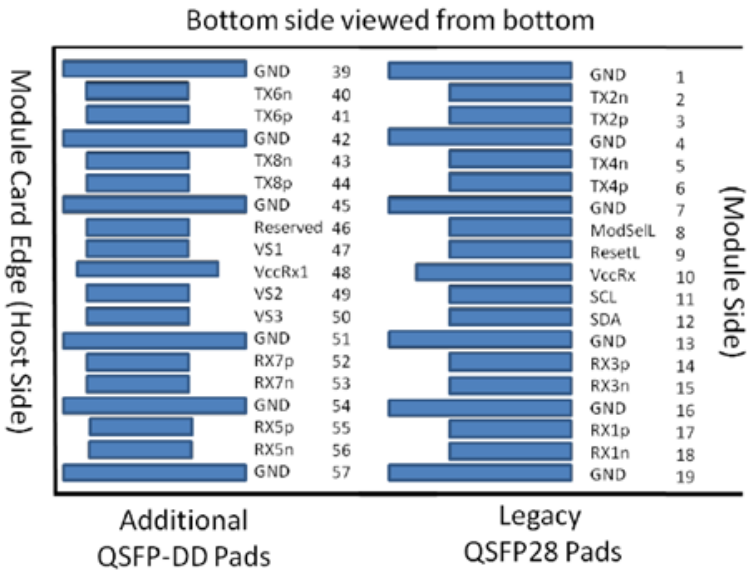


Figure 1 – Pin Definitions

Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1

Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

[1] QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence

is 1A, 2A, 3A, 1B, 2B, 3B (see Figure 2 for pad locations). Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A, 3B.

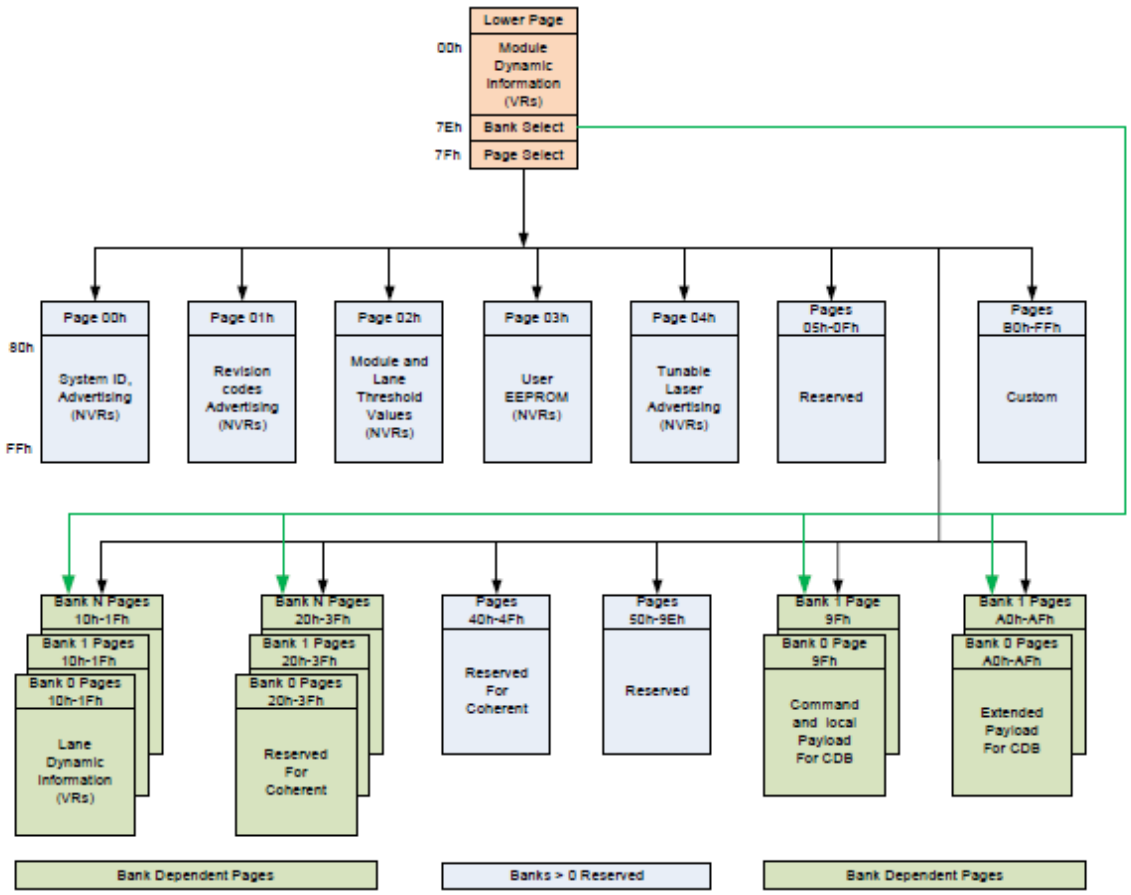
1.4 Digital Diagnostic Functions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Bit Rate (per lane)	BR		53.125		Gb/s	
Electrical Bit Error Rate (per lane)	BER			2.4E-4		PRBS31Q

1.5 Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Receiver electrical output characteristics at TP4						
Signaling rate per lane			26.5625		GBd	
AC common-mode output voltage(RMS)			-	17.5	mV	
Differential peak-to-peak output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)			0.265		UI	
Near-end Eye height, differential		70			mV	
Far-end ESMW (Eye symmetry mask width)			0.2		UI	
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage		-350		2850	mV	
Transmitter electrical input characteristics at TP1						
Signaling rate, per lane			26.5625		GBd	
Differential pk-pk input voltage tolerance		900			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
Common-mode voltage		-350		2850	mV	

1.6 Memory Map



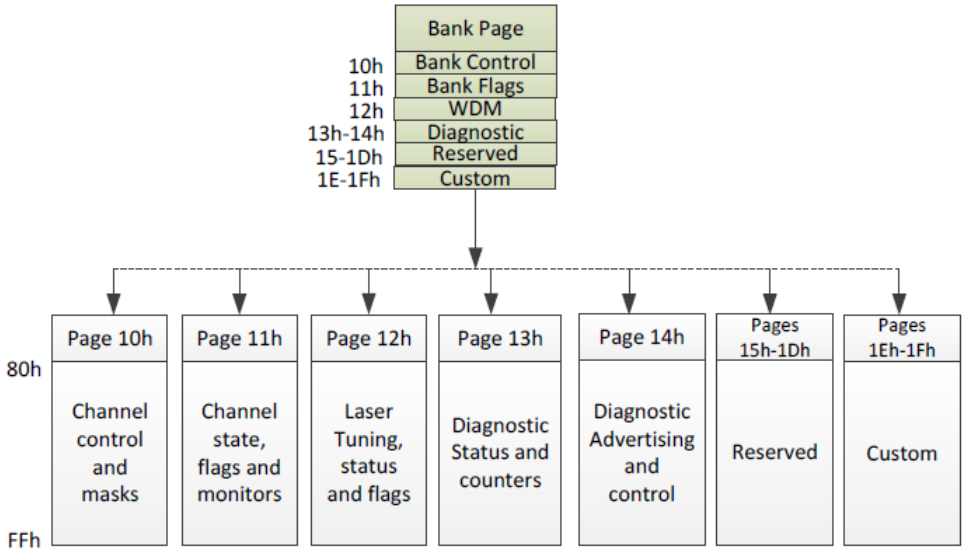


Figure 2 - QSFP-DD Memory Map

1.7 Digital Diagnostic Specification

Parameter	Symbol	Accuracy	Units	Notes
Transceiver Case Temperature	DMI_TEMP	±5	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	±3	%	Full operating range
Channel Bias current monitor	DMI_IBIAS	±10	%	Per channel
Channel RX power monitor absolute error	DMI_RX	±3	dB	Per channel
Channel TX power monitor absolute error	DMI_TX	±3	dB	Per channel

1.8 Mechanical Specifications

Unit: mm

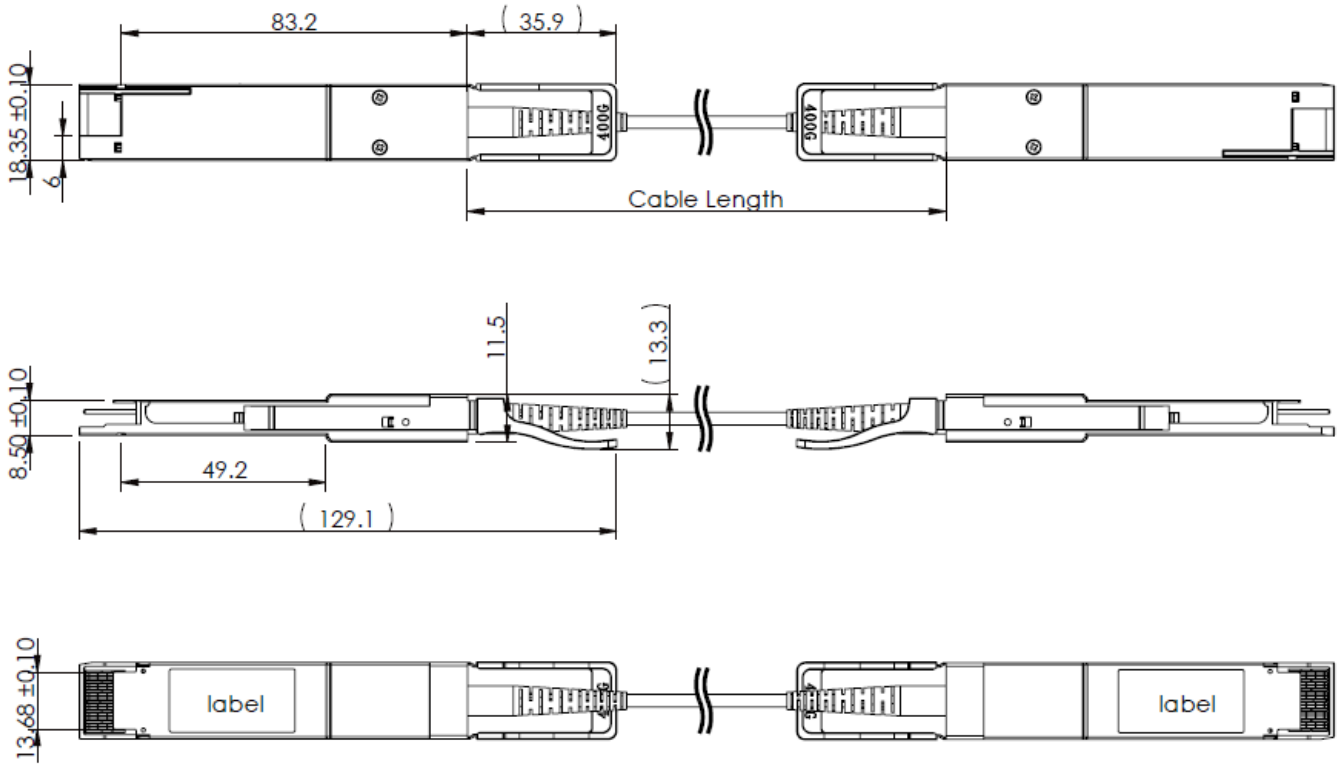


Figure 3 - Mechanical Specifications

2.0 Product Information

Data Rate	Factor		Optical	Wavelength	Reach
400G	QSFP-DD to QSFP-DD	AOC	N/A	850nm	1m~100m

ESD Safety Cautions

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Important Notice

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3.0 Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	Koko Sung	10/01/2023