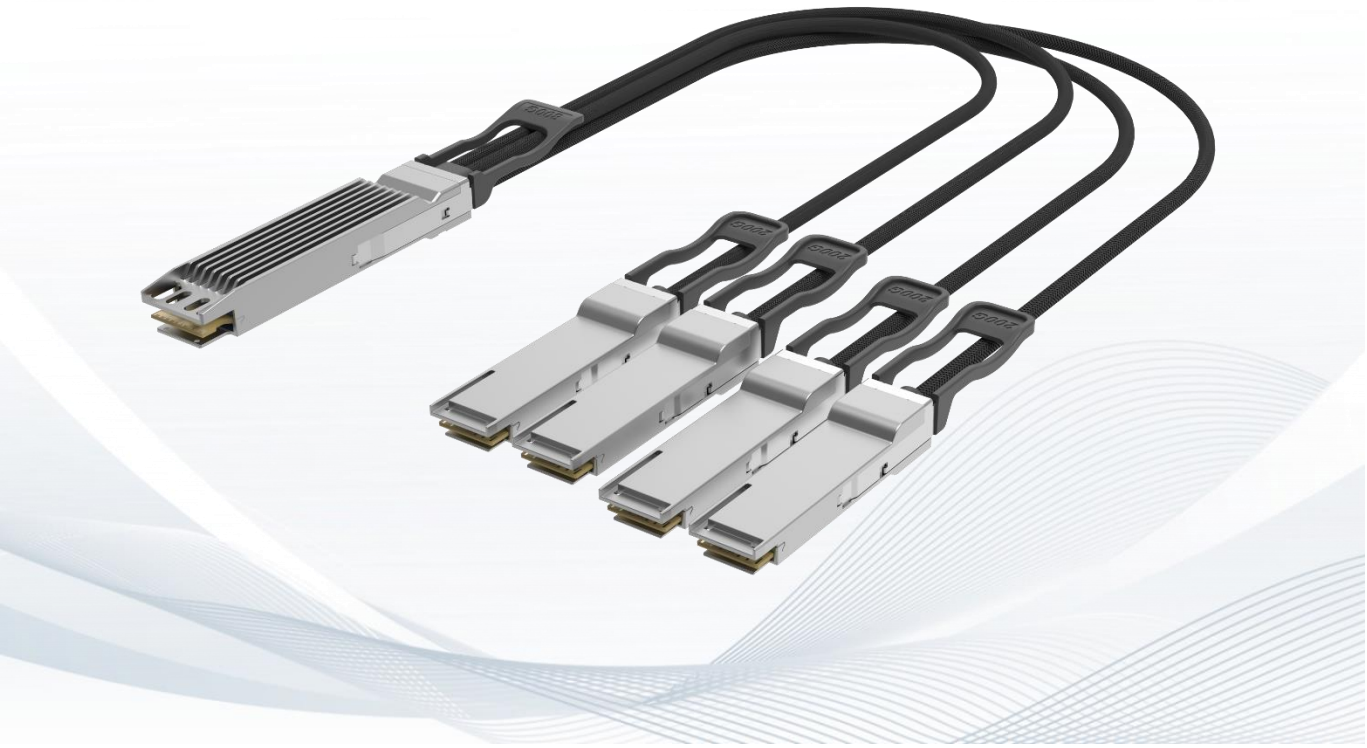
OSFP 800 to 4*QSFP112 200G Direct Attached Cable Assembly



Application

- Data Center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test And Measurement Equipment

Highlight

- Support 8x106.25G PAM4
- 800G To 4*200G Data Rate
- 3.3V Power Supply
- Hot Pluggable
- Excellent SI Performance
- RoHS Compliance
- Simplifies The Patching And Offers A Cost-Effective Way For Short Links

Standards Compliance

- Compliant with OSFP MSA Rev 4.1
- Compliant with QSFP112 MSA Rev 2.1.1
- Compliant with IEEE 802.3ck
- Compliant with IEEE 802.3cd
- I2C for EEPROM communication
- Compliant with CMIS 5.0

1.0 General Description

This datasheet pertains to the **OSFP 800G to 4*QSFP112 200G Direct Attached Copper Cable Assembly**, meticulously designed for application in the telecommunications and data center sectors. It facilitates bi-directional transmission of 2*100Gb traffic per cable, accommodating 8 lanes of 100G PAM4. The cable adheres to the standardized OSFP&QSFP112 form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 Absolute Maximum Ratings

Parameter	Unit	Min.	Max.	Notes
Supply Voltage	V	-0.3	3.6	
Data Input Voltage	V	-0.3	3.6	
Control Input Voltage	V	-0.3	3.6	
Operating Temperature	°C	0	70	
Storage Temperature	°C	-40	+85	
Relative Humidity (Non-Condensing)	%	5	85	

2.2 Operational Specification

Parameter	Unit	Min	Typical	Max	Notes
Supply Voltage (Vcc)	V	3.135	3.3	3.465	Per End
Power Consumption	W			1.5	Per End
Operating Case Temperature	°C	0		70	
Operating Relative Humidity	%	0		85	
Modulation Format		112G PAM-4			
Bit Rate	Gbps	8x100G to 4*2x100G			

2.3 Electrical Characteristics

Parameter	Unit	Min	Typical	Max	Notes
Characteristic Impedance	ohm	90	100	110	
Time Propagation Delay (Informative)	ns	.....	.....	4.9	

2.4 SI performance

Item	Parameter	Require	Reference
1	ILdd Insertion loss at 26.56 GHz	19.75 dB (Max.)	IEEE 802.3ck Section 162.11.2
2	ILdd Insertion loss at 26.56 GHz	11 dB (Min.)	IEEE 802.3ck Section 162.11.2
3	ERL Minimum cable assembly	>8.25 dB*.	IEEE 802.3ck Section 162.11.3
4	RLcd Differential-mode to common-mode return loss	0.01GHz – 40GHz Equation (162–20)	IEEE 802.3ck Section 162.11.4
5	ILcd Differential-mode to common-mode insertion loss	0.01GHz – 40GHz Equation (162–21)	IEEE 802.3ck Section 162.11.5
6	RLcc Common-mode to common-mode return loss	0.01GHz – 40GHz Equation (162–22)	IEEE 802.3ck Section 162.11.6
7	COM	3dB (Min.)	IEEE 802.3ck Section 162.11.7
*Cable assemblies with a com greater than 4 dB are not required to meet minimum ERL			

2.5 Pin Assignments

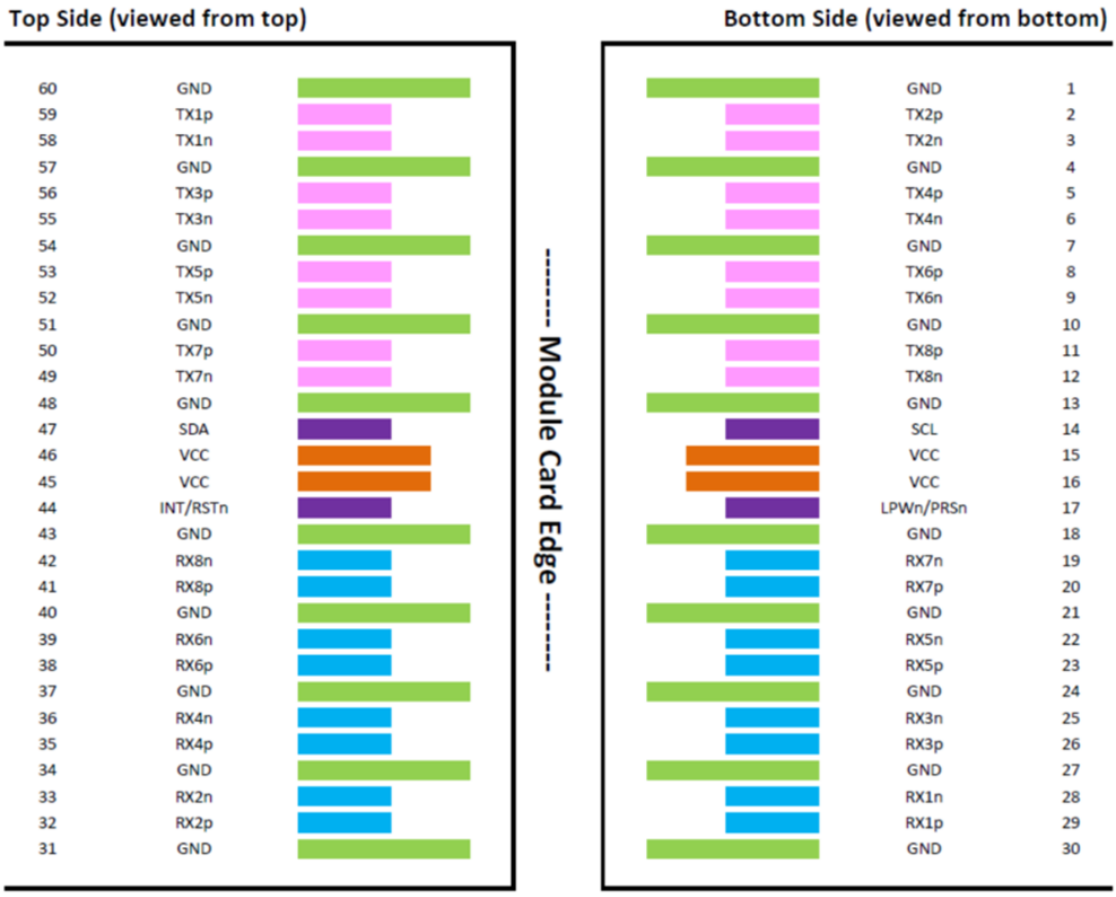


Figure 1 OSFP/OSFP RHS Type Module Contact Assignment

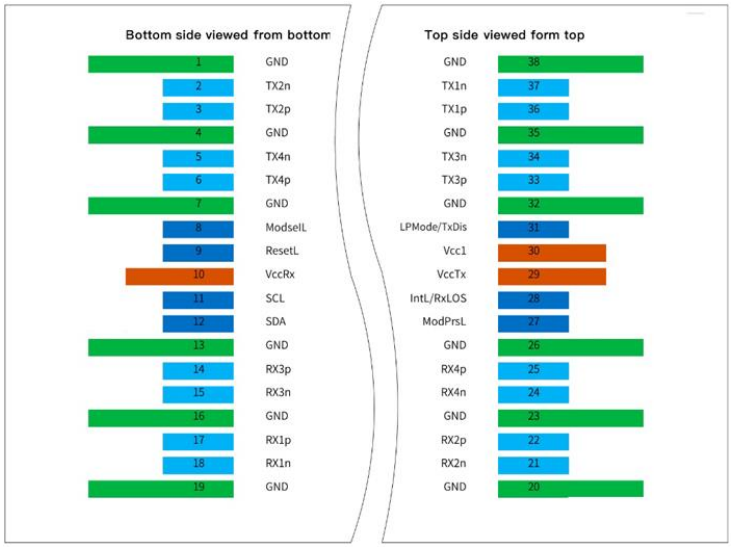


Figure 2 QSFP112 Module Contact Assignment

2.6 Pin Description

Table 1 OSFP and OSFP-RHS Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	3	
3	CML-I	TX2n	Transmitter Data Inverted	3	
4		GND	Ground	1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	3	
6	CML-I	TX4n	Transmitter Data Inverted	3	
7		GND	Ground	1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	3	
9	CML-I	TX6n	Transmitter Data Inverted	3	
10		GND	Ground	1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	3	
12	CML-I	TX8n	Transmitter Data Inverted	3	
13		GND	Ground	1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	1
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	2
18		GND	Ground	1	
19	CML-O	RX7n	Receiver Data Inverted	3	
20	CML-O	RX7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	
22	CML-O	RX5n	Receiver Data Inverted	3	
23	CML-O	RX5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	
25	CML-O	RX3n	Receiver Data Inverted	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	
28	CML-O	RX1n	Receiver Data Inverted	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	
31		GND	Ground	1	
32	CML-O	RX2p	Receiver Data Non-Inverted	3	
33	CML-O	RX2n	Receiver Data Inverted	3	
34		GND	Ground	1	
35	CML-O	RX4p	Receiver Data Non-Inverted	3	

36	CML-O	RX4n	Receiver Data Inverted	3	
37		GND	Ground	1	
38	CML-O	RX6p	Receiver Data Non-Inverted	3	
39	CML-O	RX6n	Receiver Data Inverted	3	
40		GND	Ground	1	
41	CML-O	RX8p	Receiver Data Non-Inverted	3	
42	CML-O	RX8n	Receiver Data Inverted	3	
43		GND	Ground	1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	2
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	3	1
48		GND	Ground	1	
49	CML-I	TX7n	Transmitter Data Inverted	3	
50	CML-I	TX7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	
52	CML-I	TX5n	Transmitter Data Inverted	3	
53	CML-I	TX5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	
55	CML-I	TX3n	Transmitter Data Inverted	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	
58	CML-I	TX1n	Transmitter Data Inverted	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	
Note 1: Open-Drain with pull- up resistor on Host.					
Note 2: See pin description for required circuit					

Table 2 QSFP112 Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1

8	LVTTL-1	ModseIL	Module Select	3	
9	LVTTL-1	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface clock	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Present	3	
28	LVTTL-O	Int/RxLos	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 V Power supply transmitter	2	2
30		Vcc1	3.3 V Power supply	2	2
31	LVTTL-I	LPMode/Tx Dis	Low Power Mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1:

GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module, and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane

Note 2:

Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

2.7 Cable Wiring

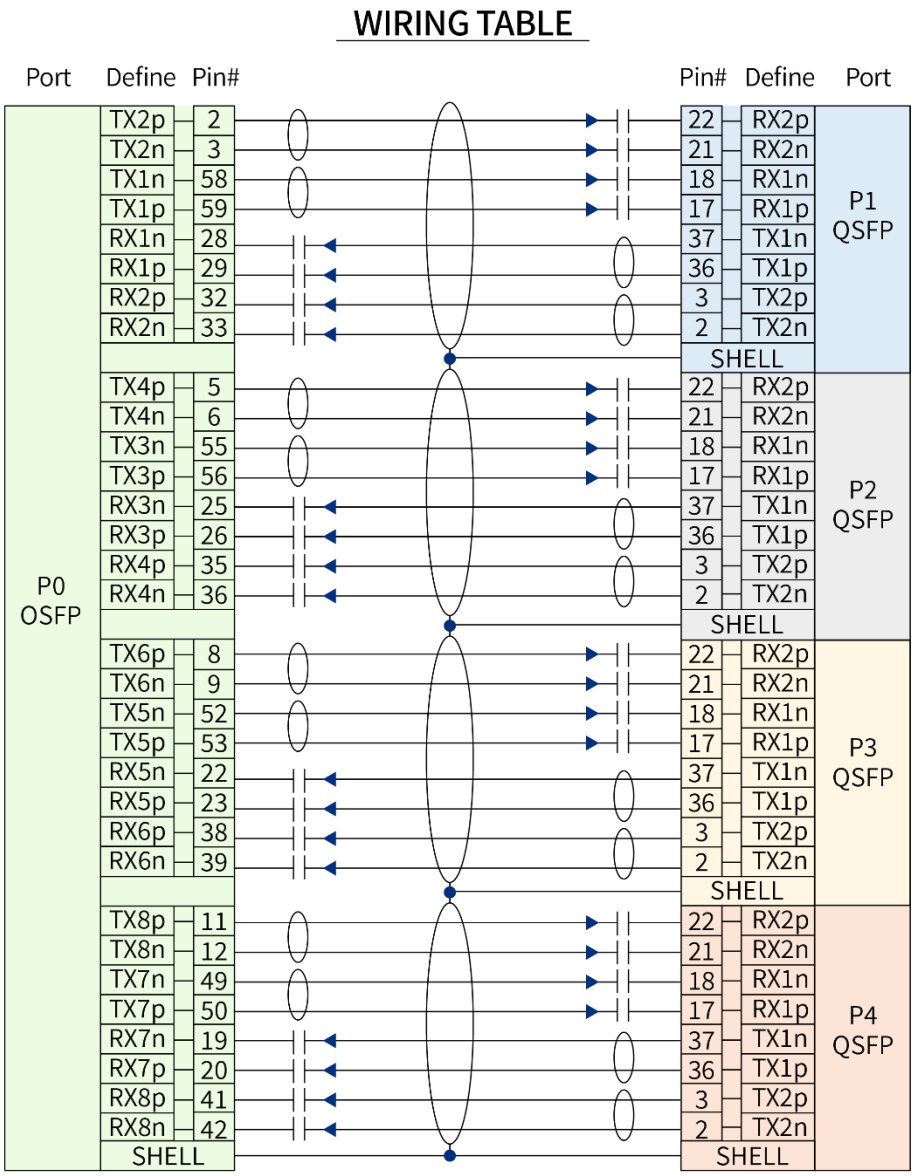


Figure 3 OSFP 800G to 4*QSFP112 (2*100G) Direct Attached Cable Assembly Wiring

2.8 Memory Map information (CMIS Version)

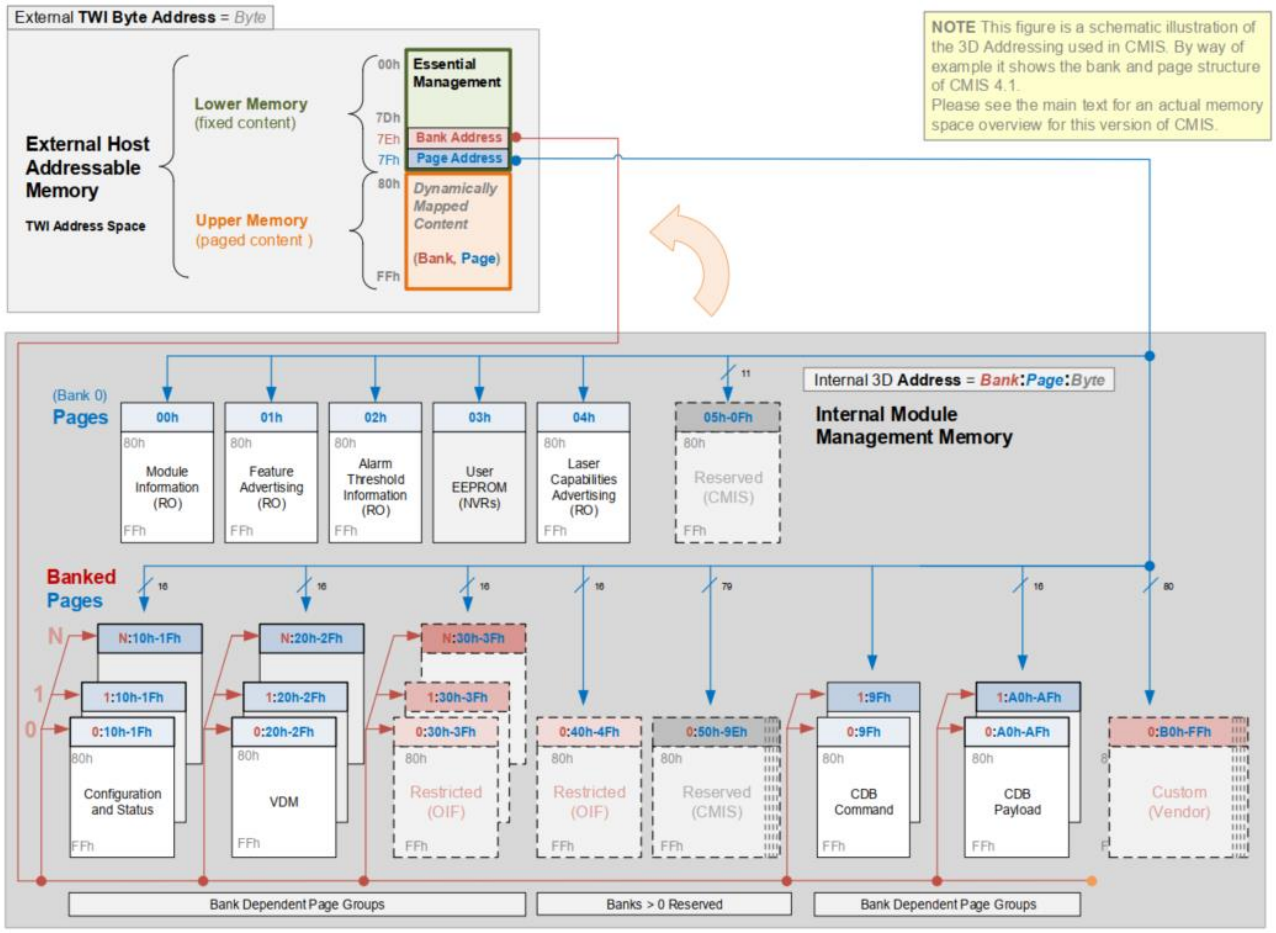


Figure 4 CMIS Module Memory Map (Conceptual View)

■ Lower Memory Overview

Address	Size	Subject Area	Description
0-3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path spedific
26-3	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version
41-63	23	Reserved Area	Reserved for future standardization

64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s）
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

■ Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII）
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Note: For the above, refer to **Common Management Interface Specification Rev5.0.**

2.9 Mechanical Specifications

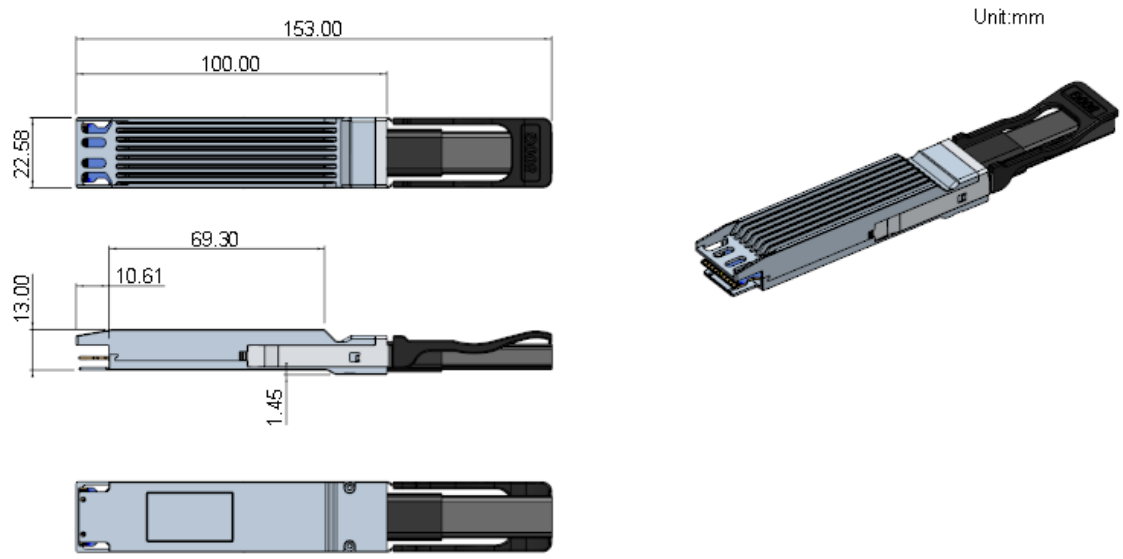


Figure 5 OSFP 800 Form Factor (P0 End)

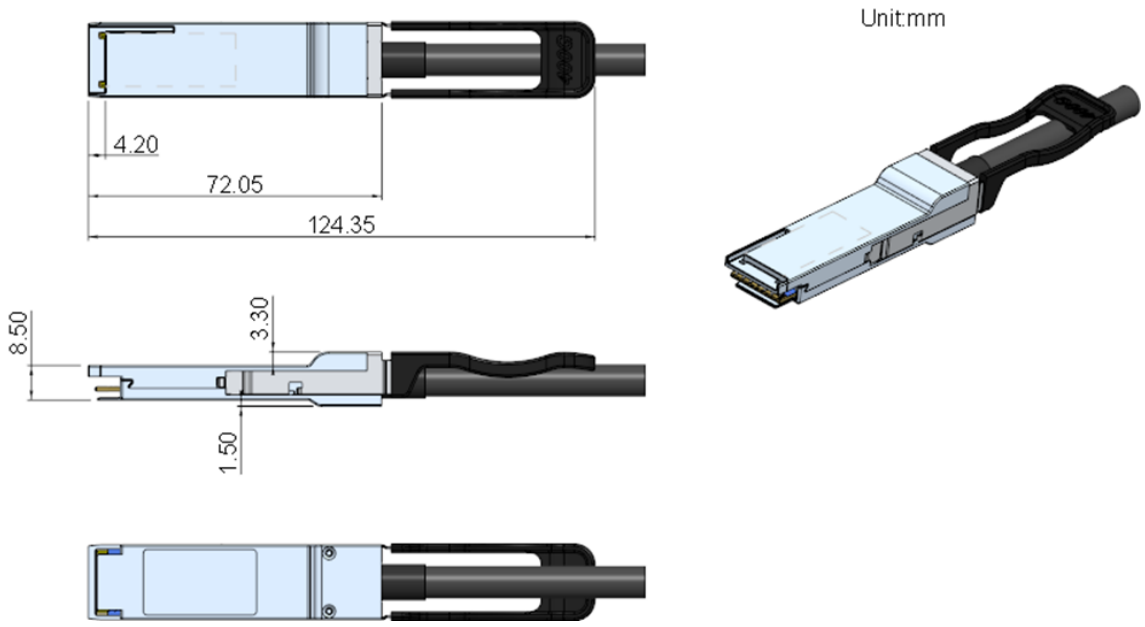
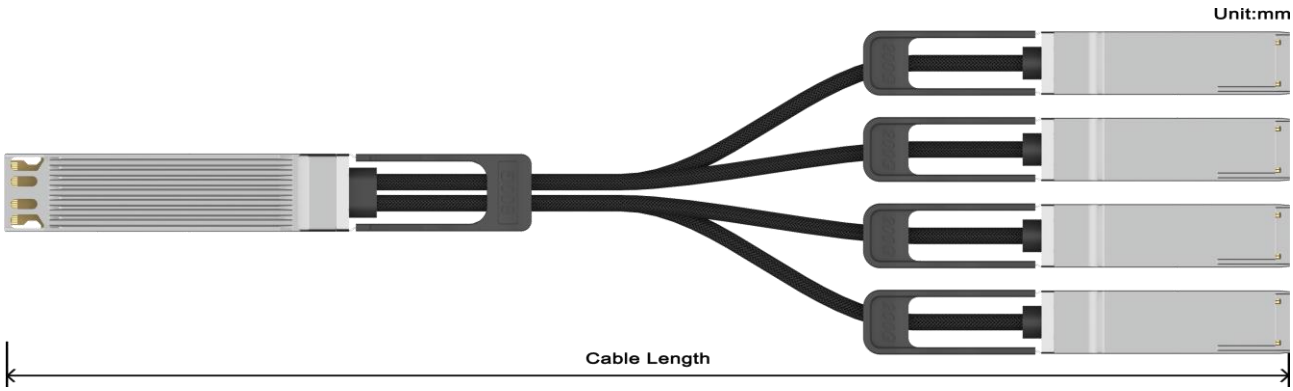


Figure 6 QSFP112 Type Form Factor (P1~P4 End)

3.0 Product Information



Product ID	Product Description	Tolerance	AWG
OSFP 800-4*QSFP112 200G-DAC-3005	OSFP(2*400G) to 4* QSFP112(2*100G) Direct Attached Cu Cable, 30AWG-0.5M	±20	30
OSFP 800-4*QSFP112 200G-DAC-3010	OSFP(2*400G) to 4* QSFP112(2*100G) Direct Attached Cu Cable, 30AWG-1.0M	±30	30
OSFP 800-4*QSFP112 200G-DAC-2815	OSFP(2*400G) to 4* QSFP112(2*100G) Direct Attached Cu Cable, 28AWG-1.5M	±40	28
OSFP 800-4*QSFP112 200G-DAC-2620	OSFP(2*400G) to 4* QSFP112(2*100G) Direct Attached Cu Cable, 26AWG-2.0M	±40	26

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4.0Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	01/16/2024