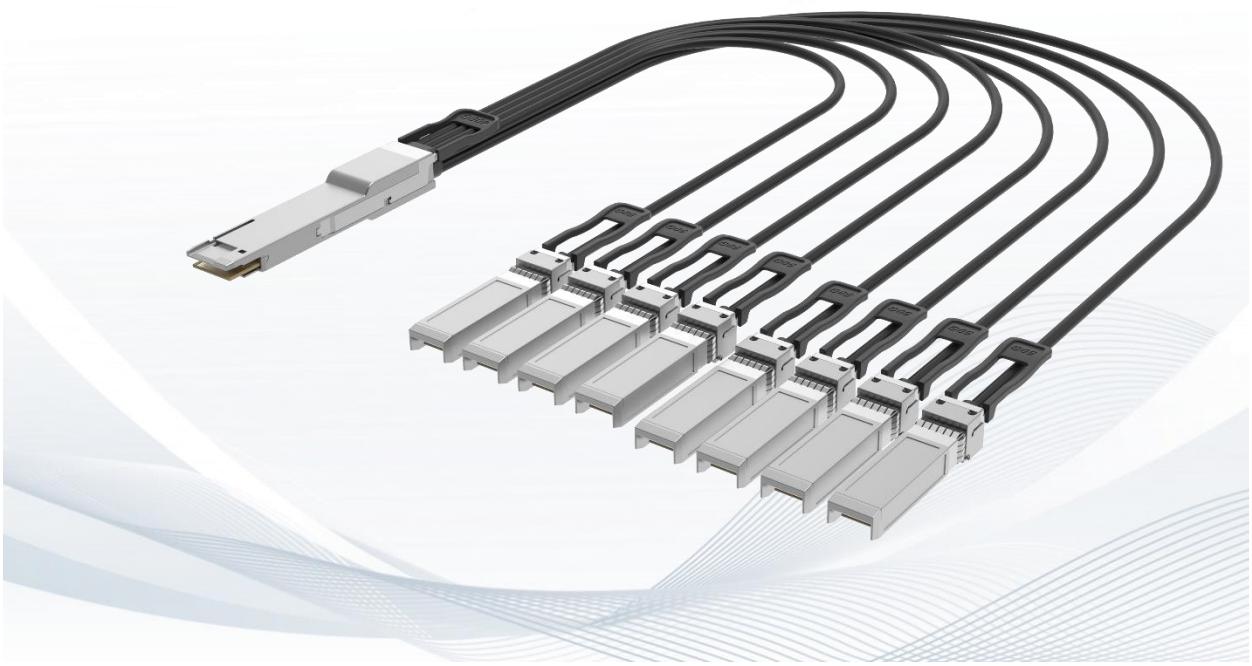


Application

- Data Center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test And Measurement Equipment

Highlight

- Support 8x56G PAM4
- 400G To 8*50G Data Rate
- 3.3V Power Supply
- Hot Pluggable
- Excellent SI Performance
- RoHS Compliance
- Simplifies The Patching And Offers A Cost-Effective Way For Short Links

Standards Compliance

- Compliant with QSFP-DD MSA Rev 4.1
- Compliant QSFP-DD-Hardware-Rev7.0
- Compliant with IEEE 802.3cd
- I2C for EEPROM communication
- Compliant with CMIS 5.0
- SFF-TA-1031,FF-8665, SFF-8661, SFF-8679, SFF-8636

1.0 General Description

This datasheet pertains to the **QSFP-DD 400G to 8*SFP56 50G Direct Attached Copper Cable Assembly**, meticulously designed for application in the telecommunications and data center sectors. It facilitates bi-directional transmission of 400Gb traffic per cable, accommodating 8 lanes of 56G PAM4. The cable adheres to the standardized QSFP-DD & SFP28(56) form factor and complies rigorously with Multi-Source Agreement (MSA) specifications.

2.0 Product Specification

2.1 Absolute Maximum Ratings

Parameter	Unit	Min.	Max.	Notes
Supply Voltage	V	-0.3	3.6	
Data Input Voltage	V	-0.3	3.6	
Control Input Voltage	V	-0.3	3.6	
Operating Temperature	°C	0	70	
Storage Temperature	°C	-40	+85	
Relative Humidity (Non-Condensing)	%	5	85	

2.2 Operational Specification

Parameter	Unit	Min	Typical	Max	Notes
Supply Voltage (Vcc)	V	3.135	3.3	3.465	Per End
Power Consumption	W			1.5	Per End
Operating Case Temperature	°C	0		70	
Operating Relative Humidity	%	0		85	
Modulation Format		56G PAM-4			
Bit Rate	Gbps	8x50G to 8*(1X50G)			

2.3 Electrical Characteristics

Parameter	Unit	Min	Typical	Max	Notes
Characteristic Impedance	ohm	90	100	110	
Time Propagation Delay (Informative)	ns	.....	.....	4.9	

2.4 SI performance

Item	Parameter	Require	Reference
1	ILdd Insertion loss at 13.28 GHz	17.16 dB (Max.)	IEEE 802.3cd Section Section 136.11.2
2	ILdd Insertion loss at 13.28 GHz	8 dB (Min.)	IEEE 802.3cd Section Section 136.11.2
3	ERL Minimum cable assembly	>11 dB*.	IEEE 802.3cd Section Section 136.11.3
4	RLcd Differential-mode to common-mode return loss	0.01GHz – 19GHz Equation (92–28)	IEEE 802.3cd Section 136.11.4
5	ILcd Differential-mode to common-mode insertion loss	0.01GHz – 19GHz Equation (92–29)	IEEE 802.3cd Section 136.11.5
6	RLcc Common-mode to common-mode return loss	0.01GHz – 19GHz Equation (92–30)	IEEE 802.3cd Section Section 136.11.6
7	COM	3dB (Min.)	IEEE 802.3cd Section Section 136.11.7
*Cable assemblies with a com greater than 4 dB are not required to meet minimum ERL			

2.5 Pin Assignments

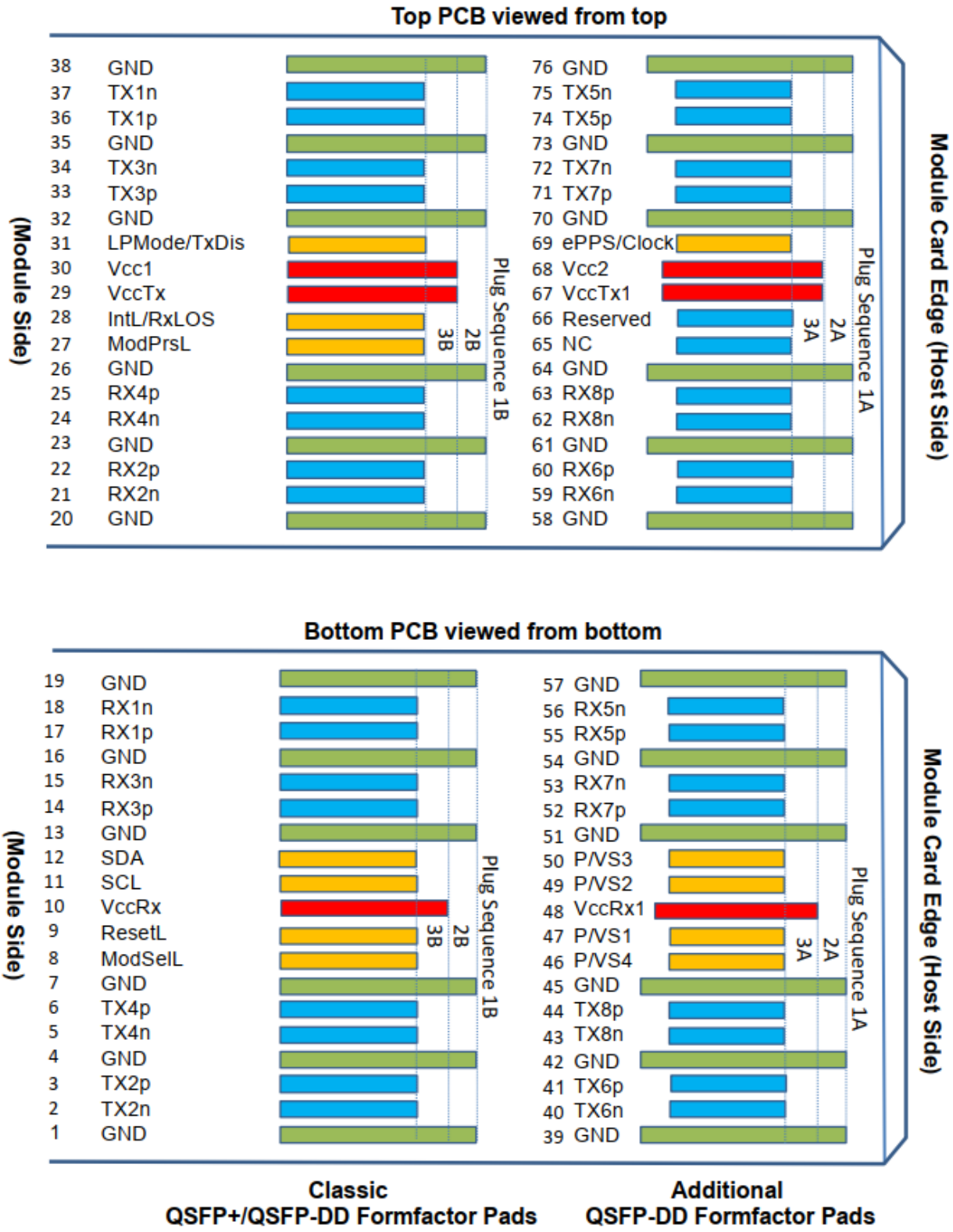


Figure 1 QSFP-DD Module Contact Assignment

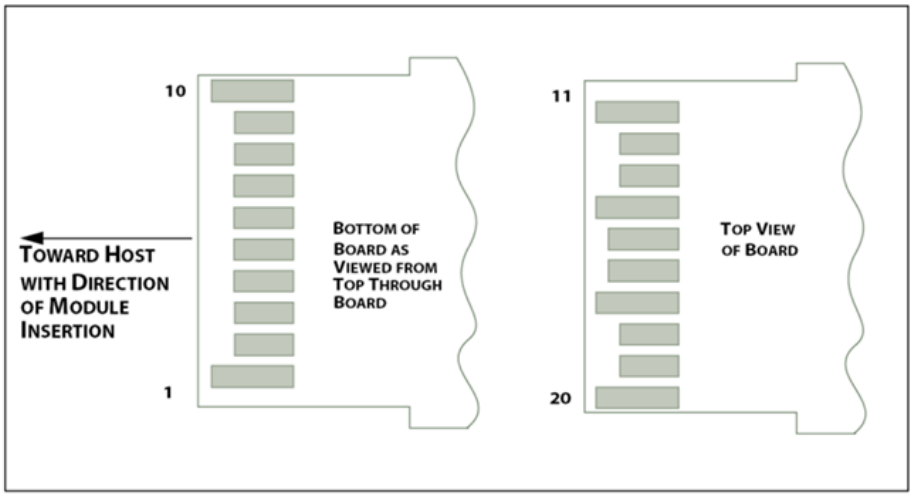


Figure 2 SFP28(56) Module Contact Assignment

2.6 Pin Description

Table 1 QSFP-DD 400 Module Pin Description

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-1		ModseIL	3B	
9	LVTTL-1		ResetL	3B	
10		Vcc Rx	+3.3V Power supply receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface clock	3B	
13		GND	Ground	1B	1
14	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx1n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	

22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Present	3B	
28	LVTTL-O	Int/RxLos	Interrupt/optional RxLOS	3B	
29		Vcc Tx	+3.3 V Power supply transmitter	2B	2
30		Vcc1	3.3 V Power supply	2B	2
31	LVTTL-I	LPMode/Tx Dis	Low Power Mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	

61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1:
QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP- DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a steady state current of 500 mA.

Note 2:
VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector(see MSA specification). For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA

Note 3:
Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.

Note 4:
Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP- DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B

Note 5:
Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

Note 6:
For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

Table 2 SFP28(56) Module Pin Description

Contacts	Logic [1]	Symbol	Power Sequence Order	Name/Description	Note
case		case	See2	Module case	
1		VeeT	1st	Module Transmitter Ground	3
2	LVTTL-O	Tx_Fault	3rd	Module Transmitter Fault	4
3	LVTTL-I	Tx_Disable	3rd	Transmitter Disable; Turns off transmitter laser output	5
4	LVTTL-I/O	SDA	3rd	2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i)	6
5	LVTTL-I/O	SCL	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)	6
6		Mod_ABS	3rd	Module Absent, connected to VeeT or VeeR in the module	7
7	LVTTL-I	RS0	3rd	Rate Select 0, optionally controls SFP+ module receiver.	8
8	LVTTL-O	Rx_LOS	3rd	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	4
9	LVTTL-I	RS1	3rd	Rate Select 1, optionally controls SFP+ module transmitter	8
10		VeeR	1st	Module Receiver Ground	3
11		VeeR	1st	Module Receiver Ground	3
12	CML-O	RD-	3rd	Receiver Inverted Data Output	
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output	
14		VeeR	1st	Module Receiver Ground	3
15		VccR	2nd	Module Receiver 3.3 V Supply	
16		VccT	2nd	Module Transmitter 3.3 V Supply	
17		VeeT	1st	Module Transmitter Ground	3
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	3rd	Transmitter Inverted Data Input	
20		VeeT	1st	Module Transmitter Ground	3

Note1:

Labeling as inputs (I) and outputs (O) are from the perspective of the module

Note2:

The case makes electrical contact to the cage before any of the board edge contacts are made.

Note3: The module signal ground contacts, VeeR and VeeT, should be isolated from the module case.
Note4: Tx_Fault is a module output that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. If Tx_Fault is not implemented, the Tx_Fault contact signal shall be held low by the module and may be connected to Vee within the module. Rx_LOS when high indicates an optical signal level below that specified in the relevant standard. Rx_LOS is an open drain/collector output, but may also be used as an input by supervisory circuitry in the module.
Note5: Tx Disable is an input contact with a 4.7 kΩ to 10 kΩ pullup to VccT inside the module.
Note6: The SFP+ 2-wire interface specifications are given in 4.2 2-WIRE ELECTRICAL SPECIFICATIONS. This specification ensures compatibility between host masters and SFP+ SCL/SDA lines and compatibility with I2C. All voltages are referenced to VeeT.
Note7: Mod_ABS is connected to VeeT or VeeR in the SFP+ module. The host may pull this contact up to Vcc_Host with a resistor in the range 4.7 kΩ to10 kΩ. Mod_ABS is asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF-8074i) this contact has the same function but is called MOD_DEF0.
Note8: RS0 and RS1 are module inputs and are pulled low to VeeT with > 30 kΩ resistors in the module. RS0 optionally selects the optical receive signaling rate coverage. RS1 optionally selects the optical transmit signaling rate coverage. The SFP+ module provides two inputs RS0 and RS1 that can optionally be used for rate selection. RS0 controls the receive path signalling rate capability, and RS1 controls the transmit path signalling rate capability

2.7 Cable Wiring

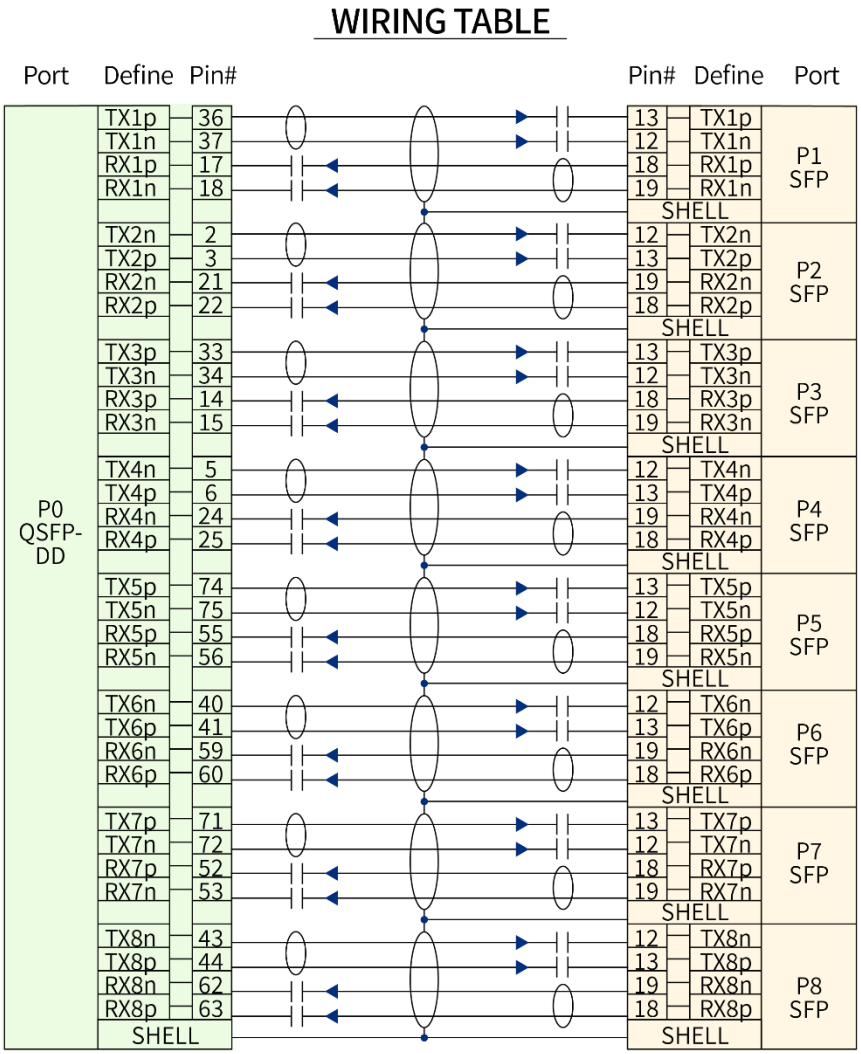


Figure 3 QSFP-DD 400G to 8*SFP56 Direct Attached cable Wiring

2.8 Memory Map information (CMIS Version)

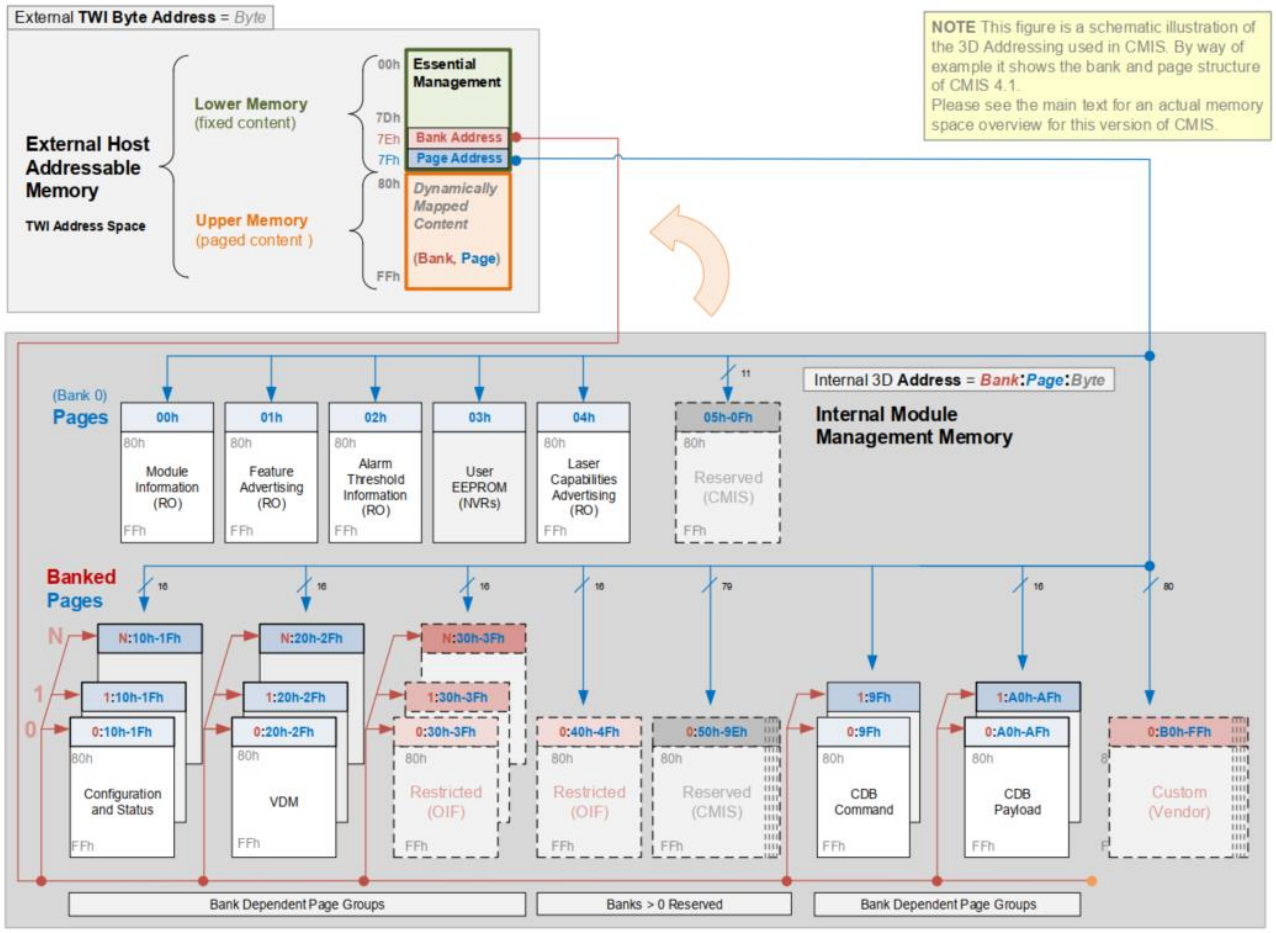


Figure 4 CMIS Module Memory Map (Conceptual View)

■ Lower Memory Overview

Address	Size	Subject Area	Description
0-3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path spedific
26-3	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version
41-63	23	Reserved Area	Reserved for future standardization

64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s）
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

■ Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII）
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Note: For the above, refer to **Common Management Interface Specification Rev5.0.**

2.9 Memory Map information (SFF-8636 Version)

Table 3 SFF-8636 Memory Map

From	To	Content	No. of bytes	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	117	Free Side Device Properties	5	Read-Only
118	118	Reserved	1	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
Upper Page 00h				
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only

2.10 Mechanical Specifications

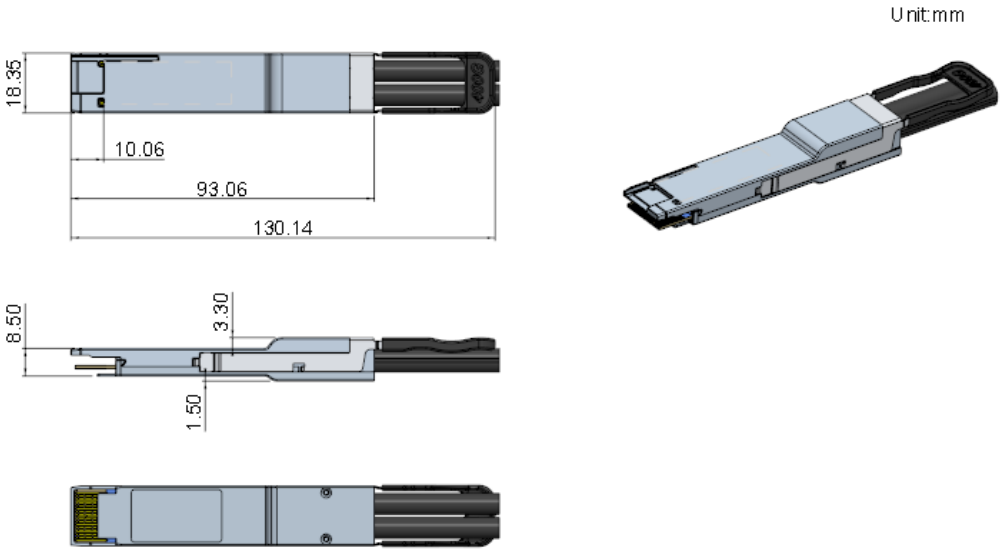


Figure 5 QSFP-DD Form Factor

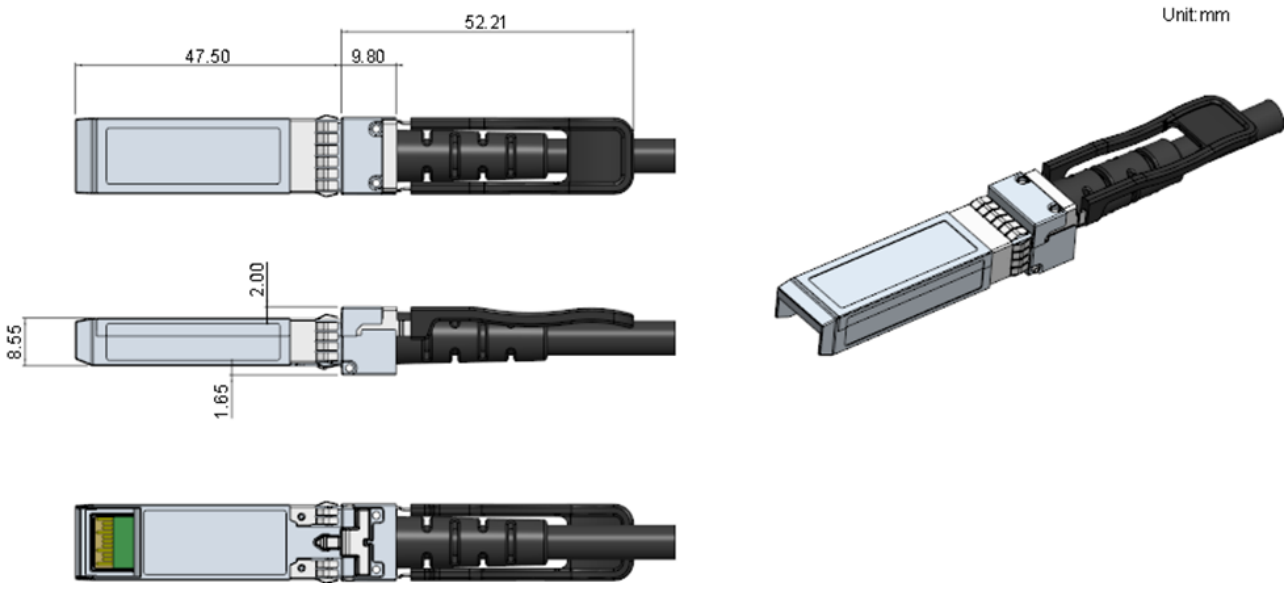
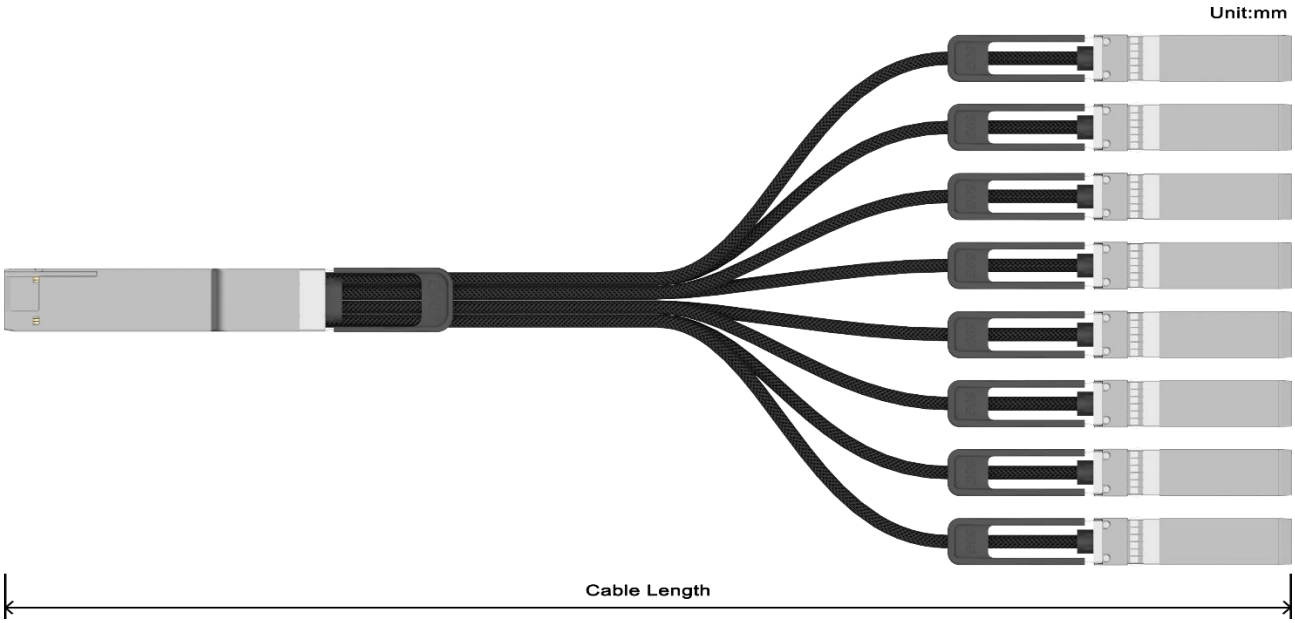


Figure 6 SFP28(56) Form Factor

3.0 Product Information



Product ID	Product Description	Tolerance	AWG
QDD-400G-8*SFP56 50G DAC-3005	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 30AWG-0.5M	±20	30
QDD-400G-8*SFP56 50G DAC-3010	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 30AWG-1.0M	±30	30
QDD-400G-8*SFP56 50G DAC-3015	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 30AWG-1.5M	±40	30
QDD-400G-8*SFP56 50G DAC-3020	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 30AWG-2.0M	±40	30
QDD-400G-8*SFP56 50G DAC-2820	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 28AWG-2.0M	±40	28
QDD-400G-8*SFP56 50G DAC-2825	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 28AWG-2.5M	±50	28
QDD-400G-8*SFP56 50G DAC-2625	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 26AWG-2.5M	±50	26
QDD-400G-8*SFP56 50G DAC-2630	QSFP-DD 400G to 8*SFP56(1*50G) Direct Attached Copper Cable, 26AWG-3.0M	±50	26

Important Notice

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4.0 Revision Record

Rev.	Comments	Author	Date
A01	Initial Release	James Chen	01/16/2024